DIGITAL CAPACITANCE MEASURING SYSTEM

FINAL REPORT

SUBMITTED IN ACCORDANCE WITH

CONTRACT NAS8-27657

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

MARSHALL SPACE FLIGHT CENTER

HUNTSVILLE, ALABAMA

MARCH 1973

2873-2143-116

SCI ELECTRONICS, INC.

A SUBSIDIARY OF SCI SYSTEMS, INC.

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PREPARED BY

SPECIAL PROJECTS SECTION

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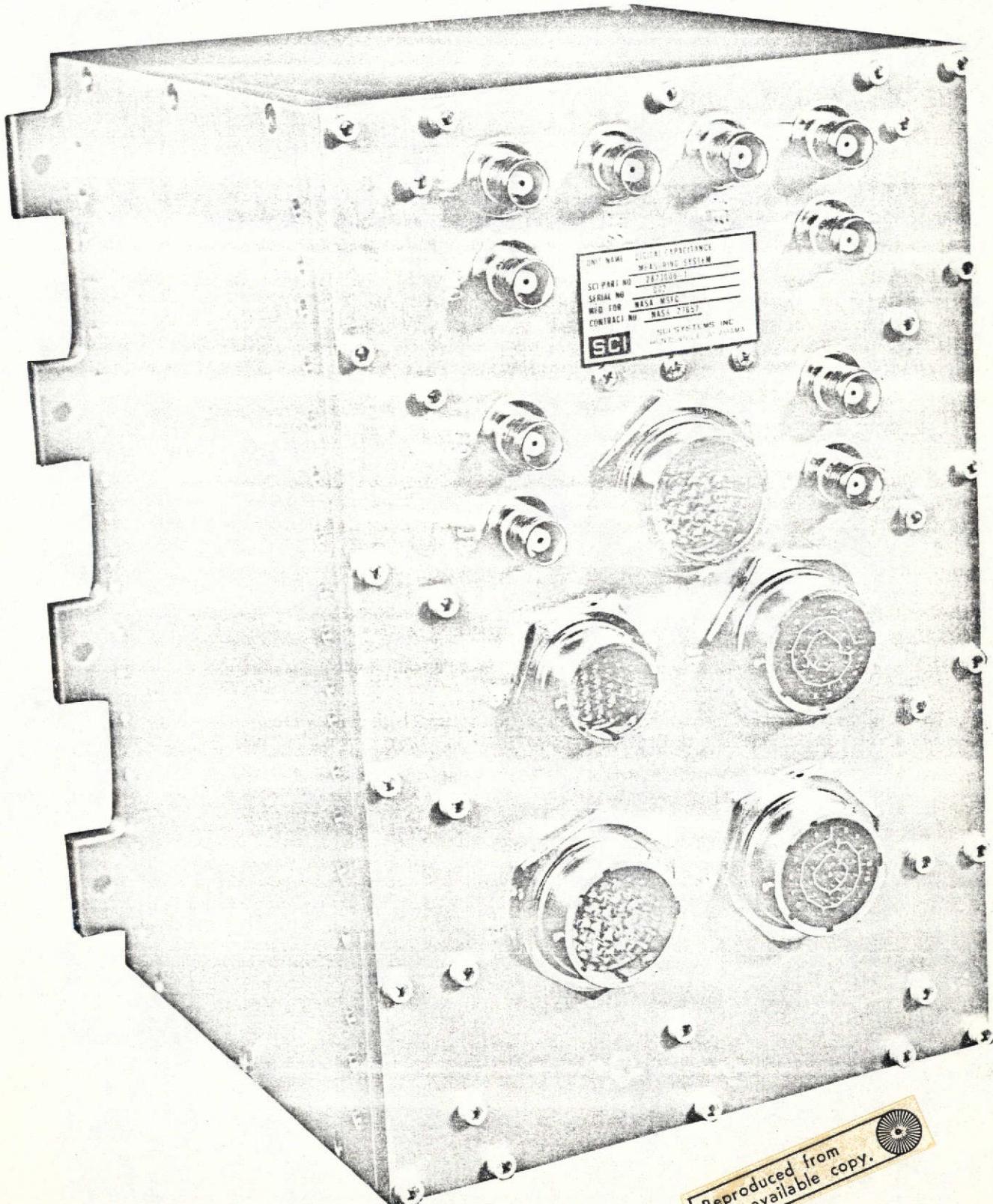
DCMS Unit

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1.0   INTRODUCTION

The final report for the Digital Capacitance Measuring System, DCMS, (Contract NAS8-27657) consists of this report and the previously submitted Phase I Report.

The Phase I report established the design definitions to be utilized in the hardware phase of this contract. Major emphasis for these definitions was placed on the DCMS interface as applicable to existing requirements for the Space Shuttle Vehicle.

This report covers the hardware phase of the contract with major emphasis on the resultant electrical design and its operation. The three units fabricated in this phase and their test results are covered.

2.0   GENERAL

The modified DCMS-200 capacitance measuring system represents major design improvements both from system capabilities and circuit improvement. The interfaces for the new system are governed mainly by Shuttle requirements.

Two major additions to the system capabilities include the addition of six discrete (point sensor) capacitance measurements and a DC/DC converter.

The six discrete capacitance measurements are performed similarly to the operation of the continuous system. A common oscillator is used for the bridge circuits for these measurements as well as the continuous bridge.

While the digital output (3 bit word) for the discrete measurements is designed for operation in conjunction with the continuous system, the discrete measurements can be operated independently using the six discrete outputs. These measurements could be used for example to quantize a capacitance measurement.

The normal range of the discrete measurements has been designed for a capacitance between approximately 4.5 and 9 pf. The threshold trip point can be set to within approximately 0.5 pf of the upper or lower range limit. The range as well as the upper and lower range limit could be changed with available bridge excitation for the discrete measurements being the limiting factor.

The internal DC/DC converter operates from a nominal 28 VDC ±15% bus. The converter provides the necessary isolation from the power bus as well as the required regulated secondary voltages. The converter design enables the DCMS unit to meet EMI flight requirements. The converter operates at

a nominal frequency of 125 kHz. Any converter noise on the secondary power lines is therefore rejected by the system even when adjusted for 90 kHz operation.

In addition to the major changes to the DCMS unit system capabilities, several minor additions were made. Changes were made in the area of internal housekeeping and operating status.

A "BITE" monitor consisting of circuitry for determining the operating condition of the three vital sub-systems, the bridge oscillator, the clock oscillator and the power converter has been added. The BITE monitor signal is available at the DCMS interface as three discrete bits representing either a GO (a logic zero) or a NO-GO (a logic one) and as a composite OPERATE/ NON-OPERATE bit.

The OPERATE/NON-OPERATE bit is a composite of the three vital subsystem monitors and the OVERRANGE and the UNDER-RANGE SIGNALS. The OPERATE/NON-OPERATE bit therefore only indicates a GO condition (logic zero) when all five inputs are in a proper operating condition. The two OVER-RANGE and UNDER-RANGE signals are also available at the interfaces as discrete bits.

In addition to the digital output, the modified DCMS Unit also provides this data as an analog output. This output has a low output impedance and can therefore be used to drive a meter.

Provisions for a sample command has been incorporated into the unit. Upon receipt of a sample command, the digital and analog output data is held in a quiescent state for the period of the sample.

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Other additions to the DCMS unit include automatic quadrature correction and differential balance adjust.

The modified DCMS also incorporates considerable expansion of the capabilities of the DCMS-200. The primary expansion being to the digital resolution and the bridge flexibility.

The modified DCMS has been expanded from a 10 to a 12 bit system. Since for certain applications the 10 bit system is still desirable, the 10 bit capability is also retained. A code plug permits the selection of the 10 or 12 bit system. To insure a full 10 or 12 bit operation, a window threshold discriminator circuit is incorporated.

The new system design provides for operation at bridge excitation frequencies from 30 kHz to 90 kHz. The DCMS-200 operated only at a bridge excitation frequency of 100 kHz. Provisions for approximately a 5% adjustment of the bridge excitation voltage has been included.

The calibrate capabilities have also been expanded. In addition to the low and high calibrates, a means for checking a full scale reading has been added. When this command is given, a fixed delta capacitance is subtracted from the actual reading. The low and high calibrates also provide a means of checking the operation of the discrete measuring system.

The redesigned DCMS unit has greater flexibility in accommodating the various modes of operation. The expanded capabilities of the unit greatly enhance its use.

3.0   THEORY OF OPERATION

3.1   GENERAL SYSTEM OPERATION

The DCMS System diagram is shown in Figure 1. The principle part of this system is the bridge network. Two signals, equal in amplitude and opposite in polarity, are applied to the bridge network by a sinewave oscillator. An unbalance in the bridge components establishes two currents, one the reference current and the other, the unknown current. These currents are transformer coupled to a summing amplifier which establishes an error signal. This error is filtered and amplified, then it is compared to the oscillator signal (shifted about 90 degrees) in a phase detector. The output of the phase detector causes the up-down counter to count one bit in a direction which will tend to distribute the reference current in the summing amplifier so as to oppose the unknown current. The current summation is accomplished with a resistor R2R ladder network producing currents of 1/2, 1/4.....1/4096. The up-down counter continues to count and the fractional currents are compared one at a time until the net output of the summation amplifier is zero. The output of the up-down counter provides the digital display of the ratio between the reference and unknown capacitances. Analog data derived from this digital display is also available as an output. The system diagram also shows the point sensor circuit, which produces a 3 bit word from six discrete probes.

3.2   DETAILED THEORY OF OPERATION

3.2.1   Oscillator

Drawing 2873J53 is a schematic of the oscillator and amplifier. Transistors Q1 and Q2 drive transformer T1 which forms a high -Q LC oscillator to provide a low distortion sinewave output. Transistor Q3 is used to maintain a constant output amplitude with low distortion. Diode CR1 rectifies the

FIGURE I

Point Sensor Quadrature

Point Sensor Calibrate

Point Sensor No. 2

Shield

Point Sensor No. 1

Shield

High Level Simulate

Full Probe Test

Oscillator

Shield

Quadrature Reference

Detector Phase Adjust

In-Phase Reference

Differential Balance Adj.

Quadrature Unknown

Bridge Network Board

Shield

Window Threshold

In-Phase Unknown

Phase Detector

Shield

Error Amp. Gain Adjust

Filter Error Amplifier

Shield

Low Level Simulate

ADC Gain Adjust

ADC/DAC

Shield

Up-Down Counter No. 2

Up-Down Counter No. 1

Shield

Power Supply

Printed Circuit Board and Potentiometer Location
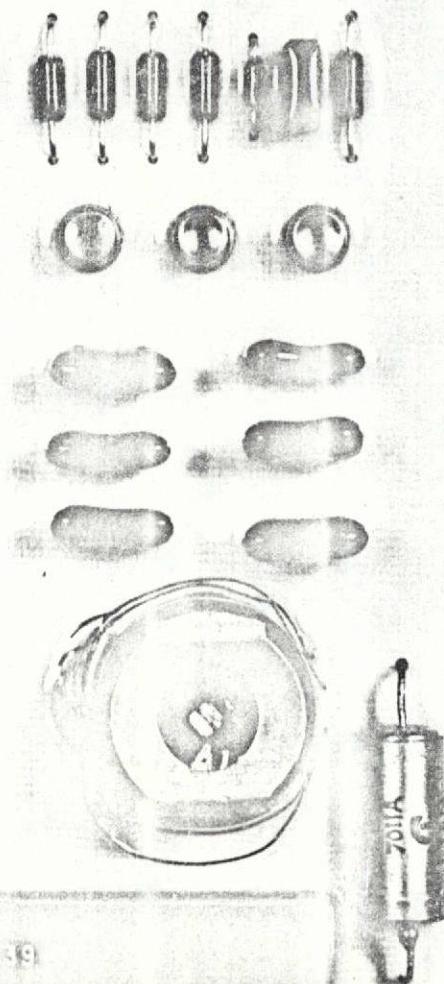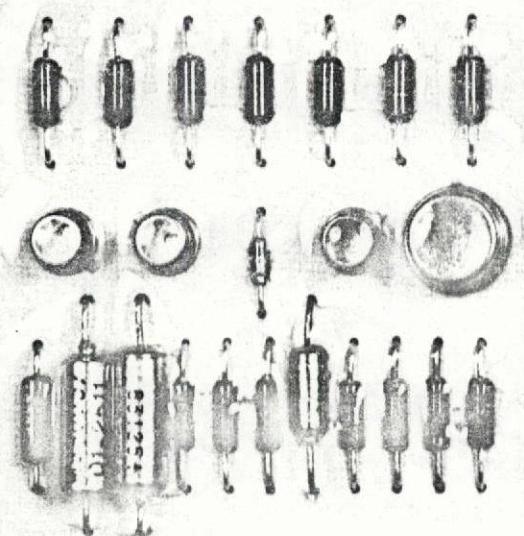
Photograph   Oscillator
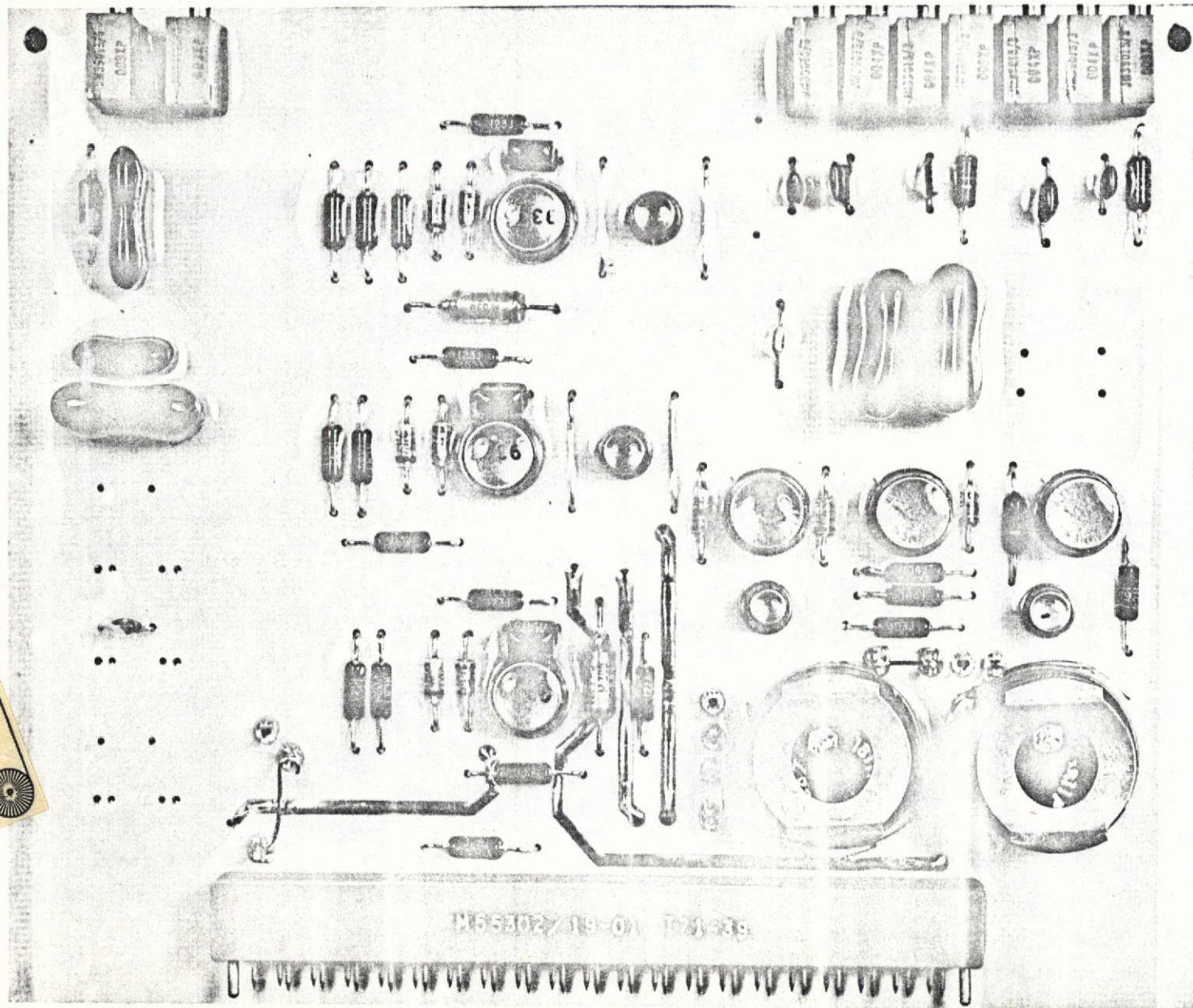
Photograph   Bridge Network Board

oscillator output to control the on resistance of Q3. If the oscillator output drops, this lowers the voltage on the gate of Q3 and this lowers the drain to source resistance of Q3 causing the oscillator amplitude to rise back to the proper output level. The oscillator drives the power amplifier from secondary winding No. 11 and 12.

The power amplifier consists of three pairs of differential amplifiers to provide 50 volts peak-to-peak to drive long lengths of cable with low distortion. The amplifier output transformer provides 5 sets of secondary output windings to drive the bridge network and also for the point sensor circuit. Output winding 9, 10-11, and 12 provide $\pm$ 50 volts peak-to-peak to drive the bridge. Output winding 13, 14-15, and 16 provide $\pm$ 5 volts to drive the differential adjust potentiometer. Winding 17, 18-19 and 20 provide about $\pm$ 17 volts peak-to-peak to excite two phase shift networks, one for the main probe and one for the point sensor circuit. Winding 21, 22-23 and 24 provide about $\pm$ 2.5 V peak-to-peak to five 100 ohm and two 5K ohm potentiometers to provide seven voltage sources for trimming and nulling the bridge. Output windings 25 through 30 provide a total of about 7.5 volts peak-to-peak to drive the point sensor circuitry.

Transistor Q6-Q7 is the input differential amplifier which drives the power output differential stage Q9-Q10. AC feedback is provided by T2 winding 5 and 6 and resistor R17 for low distortion and stable gain. Winding 7 and 8 provide about -5 volts for operation of Q8. Transistors Q4, Q45, and Q stabilizes the DC operating point of the amplifier to provide low distortion and a stable DC operating point. The base of Q8 gets negative DC feedback from the collector of Q4. The output stage transistors are mounted on the DCMS housing top plate for an effective heat sink.

3.2.2 Bridge Network Board

Drawing No. 2873032 is a schematic of the bridge network. The most common application of the DCMS is the measurement of absolute capacitance. For the measurement of absolute capacitance, a 50 volt peak-to-peak signal, E+ and E- is applied to the bridge as shown in Figure 2. Voltages E+ and E- are 180° out of phase.

Capacitors C21-C22 in the bridge are used to establish a reference for the initial value of the external transducer which is C15 and C16. Capacitors C17-C18 are used as a reference for the total value of change of the external transducer. For this circuit configuration, C19 and C20 are not used.

When the external transducer is equal in capacitance to C21 and C22, E+ and E- cancel each other at point A and there is no current flow in the primary winding of T1. As the capacitance of transducer C15-C16 is increased, current will flow in the primary of T1, and will increase linearly with the capacitance increase of C15-C16. To measure this current, it is coupled to the summing amplifier where it is compared with a selected fraction of the reference current. The reference current in transformer T2 is caused by reference capacitor C17-C18. Components R23, C13, R25 and C14 are used to calibrate the DCMS to the initial and total values of the external transducer.

The bridge works primarily the same for capacitance difference and capacitance ratio. The only change is in the component configuration.

The DCMS is also capable of measuring the ratio of the capacitance of two external transducers as in the case of a liquid level probe. The probe consits of two variables, a reference and an unknown. The operation of this function is as follows:
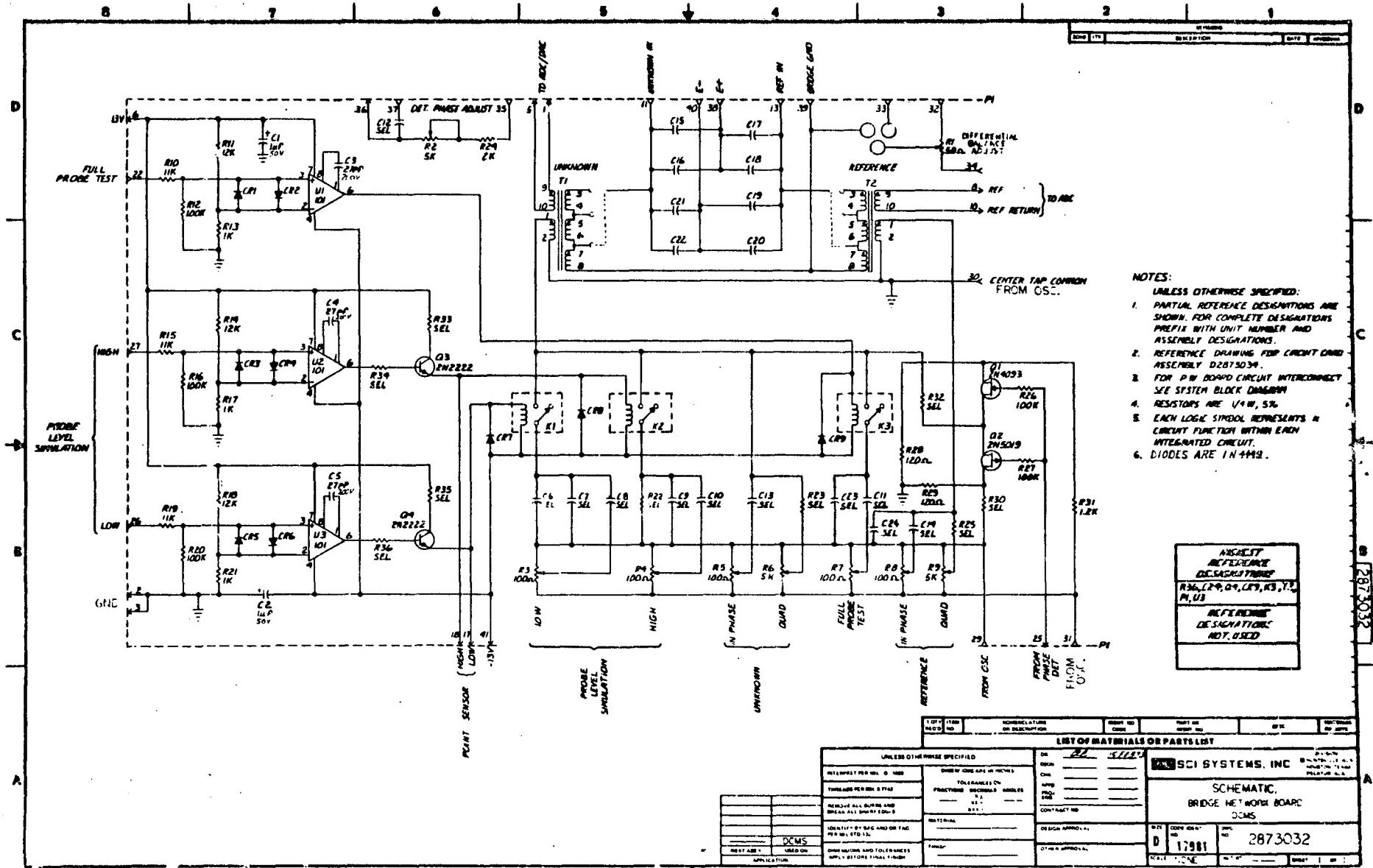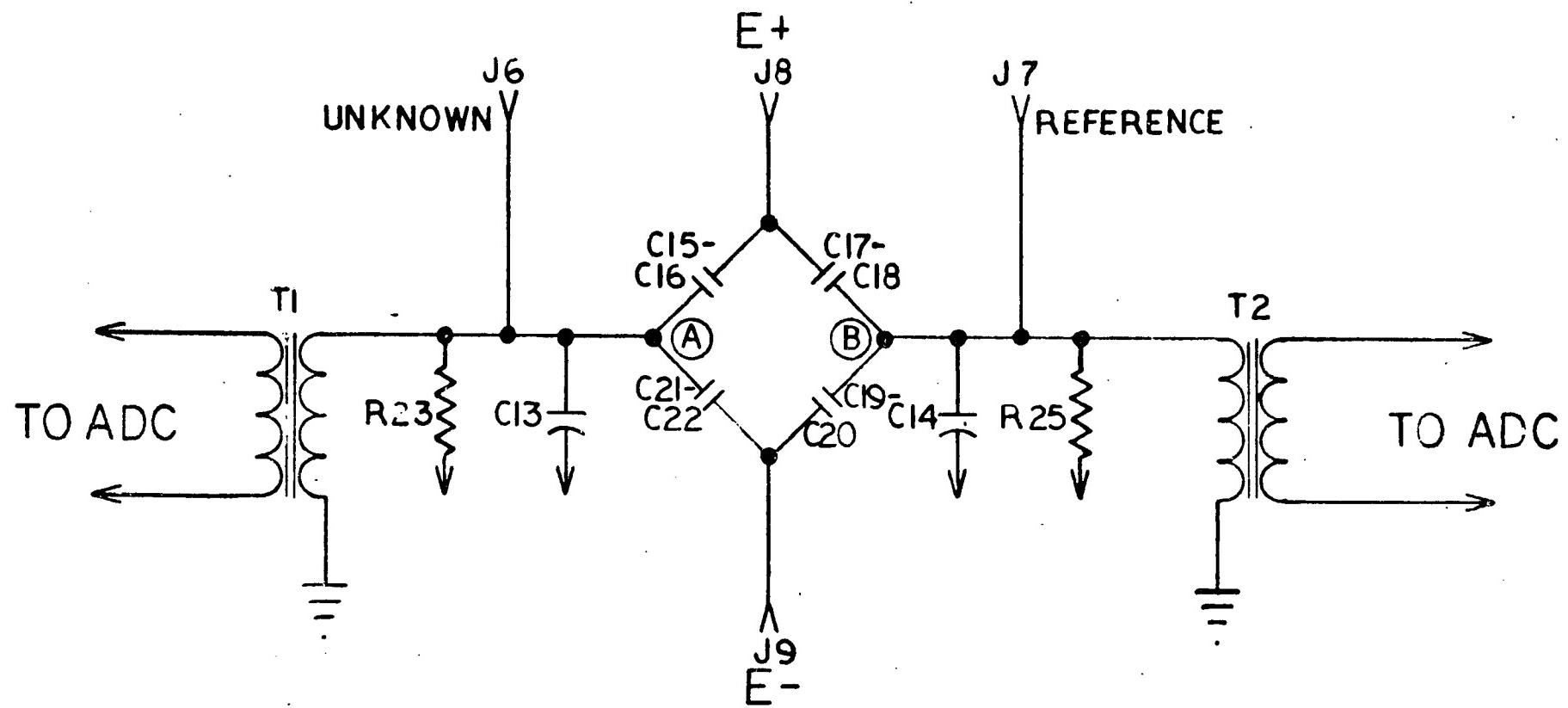
SCHEMATIC,
BRIDGE NETWORK BOARD
DCMS

2873032

FIGURE 2

SIZE	CODE IDENT	DWG	
A	NO. 17981	NO.	FIGURE 2
SCALE		UNIT WT.	SHEET OF
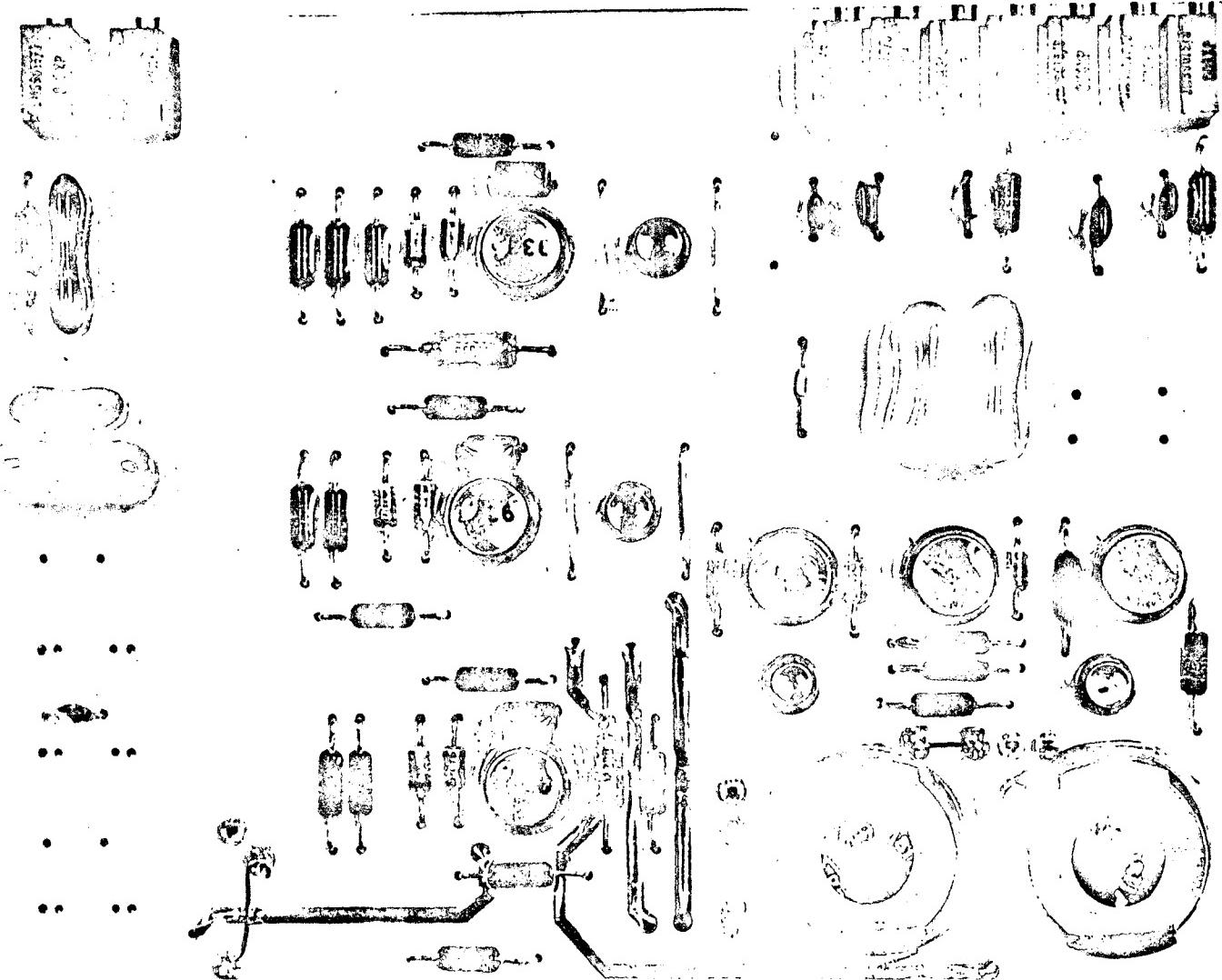
Photograph   Bridge Network Board

Referring to Figure 2, C17-C18 is the reference variable and C15-C16 is the unknown variable. C19-C20 is fixed at the initial value of C17-C18. Capacitor C21-C22 is fixed at the initial value of C15-C16. When C17-C18 and C15-C16 are at their initial values, points A and B are balanced and there is no current flow in either transformer primary winding.

As the probe is filled with liquid, it must first change the dielectric of C17-C18 to its absolute value. This change unbalances point B and causes current flow in the primary winding of T2 which is coupled to the R2R ladder network of the ADC. This establishes a constant reference current. At this point, no liquid has yet been introduced between the plates of C15-C16 and point A is still balanced with no current flow in T1. This point is the zero level, as the liquid continues to rise, it causes a dielectric change between the plates of C15-C16 creating an unbalance at Point A. It is this unbalance that causes a current to flow in the primary winding of T1.

To establish a comparison of the two external capacitances, the current may be attenuated to the degree desired. For example, if the maximum capacitance of the transducers have a ratio of 20:1, the amount of unknown current coupled into the summing junction must be attenuated to 1/20 of the current flowing in the secondary winding of T1. This is accomplished by a divider network in the secondary winding of T1, consisting of R67 and R87 on schematic drawing 2873026.

Any variation of the level of liquid between the plates of C15-C16 causes a capacitance change that is a function of the total change of C15-C16 and is proportional to the change in C17-C18. This unknown change in C15-C16 creates the unknown current which, when properly attenuated in the secondary of T1 is coupled to the input of the summing amplifier. Here it is programmed by the 12 bit counter. The state of the 12 bit counter then provides a digital display of the ratio of the two currents.

In order for the DCMS to measure capacitance difference, there must be two external variable capacitors such that each capacitor is subject to all the variables of the other. There must also be an internal reference capacitor which is equal to twice the difference to be resolved between the two external transducers.

Referring to Figure 2, C17-C18 is selected as the internal reference capacitor while C21-C22 and C15-C16 are the external transducers. In this application, C19-C20 is omitted to establish a constant unbalance at Point B. This unbalance causes a constant reference current at Point B which is coupled across T2 to the reference input of the ladder network in the ADC. When C21-C22 and C15-C16 are equal in capacitance, Point A is balanced and there no error current in the primary of T1. By inserting a capacitor in parallel with C15-C16, equal to 1/2 the value of C17-C18, there is established a half-scale offset when C21-C22 a d C15-C16 are equal. This error sets the 12-Bit Counter in the 100--0000 half-scale state.

When there is a capacitance difference between C21-C22 and C15-C16 equal to 1/2 the capacitance of C17-C18 with C21-C22 the larger capacitance, the counters are set in the 000---01 state. With the same difference, and C15-C16 the greater capacitance, the counters will be in the 111--11 or full-scale state. The system is thereby enabled to interpret a positive or negative difference of C15-C16 and C21-C22 up to plus or minus one-half the value of C17-C18.

Transformers T1 and T2 provide input ground isolation from the DCMS common ground and also provide a very low input impedance to the bridge currents. Taps are provided on the primaries of T1 and T2 to allow impedance selection. The load on the secondaries is always about 1K. This is transformed down to 5 ohms at the lowest tap, 20 ohms at the second

tap, and 45 ohms at the highest tap. Of course, the higher the input impedance the greater the power developed at the point and the better the signal to noise ratio. The bridge network accepts unbalance currents from outside the unit via J6 and J7.

In the secondary of th "unknown" coupling transformer T1, an attenuation circuit is provided to attenuate the unknown current in order to make the full scale ratio equal to or less than 1.0. The selected resistors are R67 and R87 shown in Drawing 2873026. R88 is a 50 ohm potentiometer which allows fine calibration of full scale. In all cases, the parallel value of R67 and R87 should be 1K $\pm$ 10% in order to equalize the input impedance at the two inputs.

Three relays are provided which connect in or command currents which are designed to simulate a change in the bridge components. The relays are made to energize with a remote command. Amplifiers U1, U2 and U3 are used to drive simulate relays from worst case TTL voltage levels, which are applied to the three inputs pins 22, 26 and 27. Input resistor R10, CR1 and CR2 form an overvoltage protection circuit for the input of U1. Amplifiers U2 and U3 are likewise protected. Amplifiers U2 and U3 have emitter follower outputs to drive an additional relay each, these relays are located on one of the point sensor circuit boards.

A $90°$ phase shift network is composed of C12, R2, and R24. Its output (Pin 36) goes to the in-phase detector.

Transistors Q1 and Q2 are part of the automatic quadrature null circuit. A DC control voltage from the bridge phase detector circuit board (Drawing No. 2873035) is used to control the on resistance of FET Q1 or Q2. Therefore, the amount of oscillator voltage injected into T1 may be controlled.

A positive voltage on Pin 25 will tend to turn Q2 off, allowing the oscillator signal to pass through Q1. A negative voltage on Pin 25 will tend to turn Q1 off, allowing the oscillator signal to pass through Q2. This DC control voltage is produced by a quadrature phase detector to detect any quadrature component of the error signal. This control voltage is feedback to Q1 and Q2 to reduce the quadrature component to an acceptable level.

3.2.3   ADC/DAC (Summing Amplifier Circuit)

Drawing No. 2873026 is a schematic of the ADC/DAC circuit. This circuit accepts the unknown and reference signals from the bridge, performs the summing function, produces an error output signal, a DC reference voltage of 5 volts, and a DC analog output voltage of zero to 5 volts.

The DC portion of this circuit will be considered first. Operational amplifier AI and its associated circuit are used to generate a very stable 10 volt DC reference voltage. Start-up of this circuit is provided by voltage divider R4 and R5, this bias is coupled to the operational amplifier non-inverting input through diode CR1 (after the circuit is in regulation CR1 reverse biases). The small start-up bias from CR1 to the input causes the output (Pin 6) to rise also. Positive feedback is provided by R6 and the gain of A1 is greater than unity (about 1.7). With positive feedback, A1 output rapidly rises to about 6.2 volts. At this point, temperature compensated zener diode VR1 starts to conduct and clamp the non-inverting input (Pin 3) to 6.2 volts. At this point, the inverting input (Pin 2) has a potential of about +3.6 volts. This is due to the divider network R1, R2, R3, R8, R89 and R90. Since the non-inverting input is about 2.6 volts, more positive than the inverting input, the output will continue to rise until it reaches 10 volts. When the output reaches 10 volts, Pins 2 and 3 will be equal and maintain 10 volts output. This circuit rejects supply voltage changes and is very stable with temperature.

SCHEMATIC
ADC/DAC,
DCMS

2873026
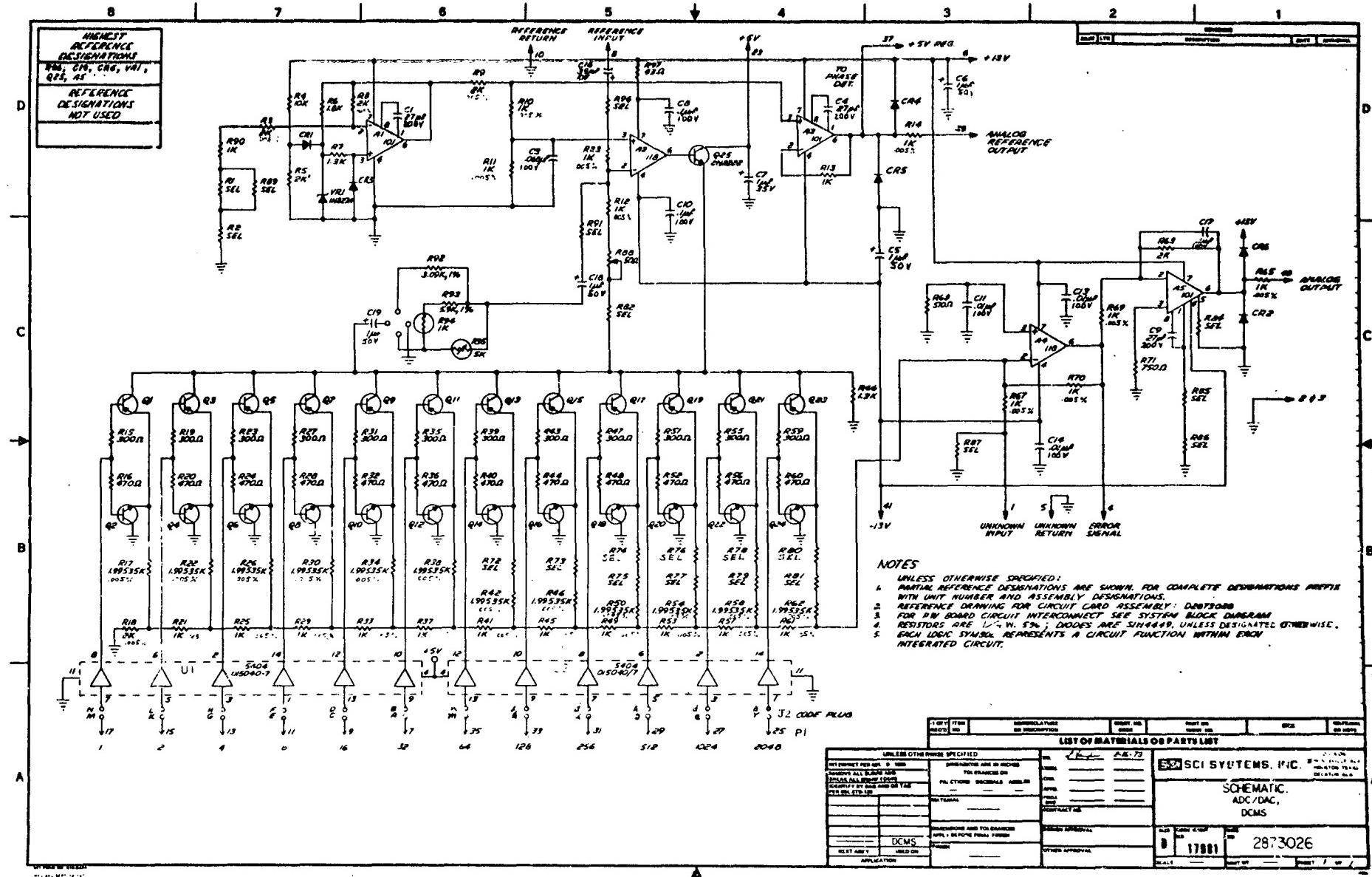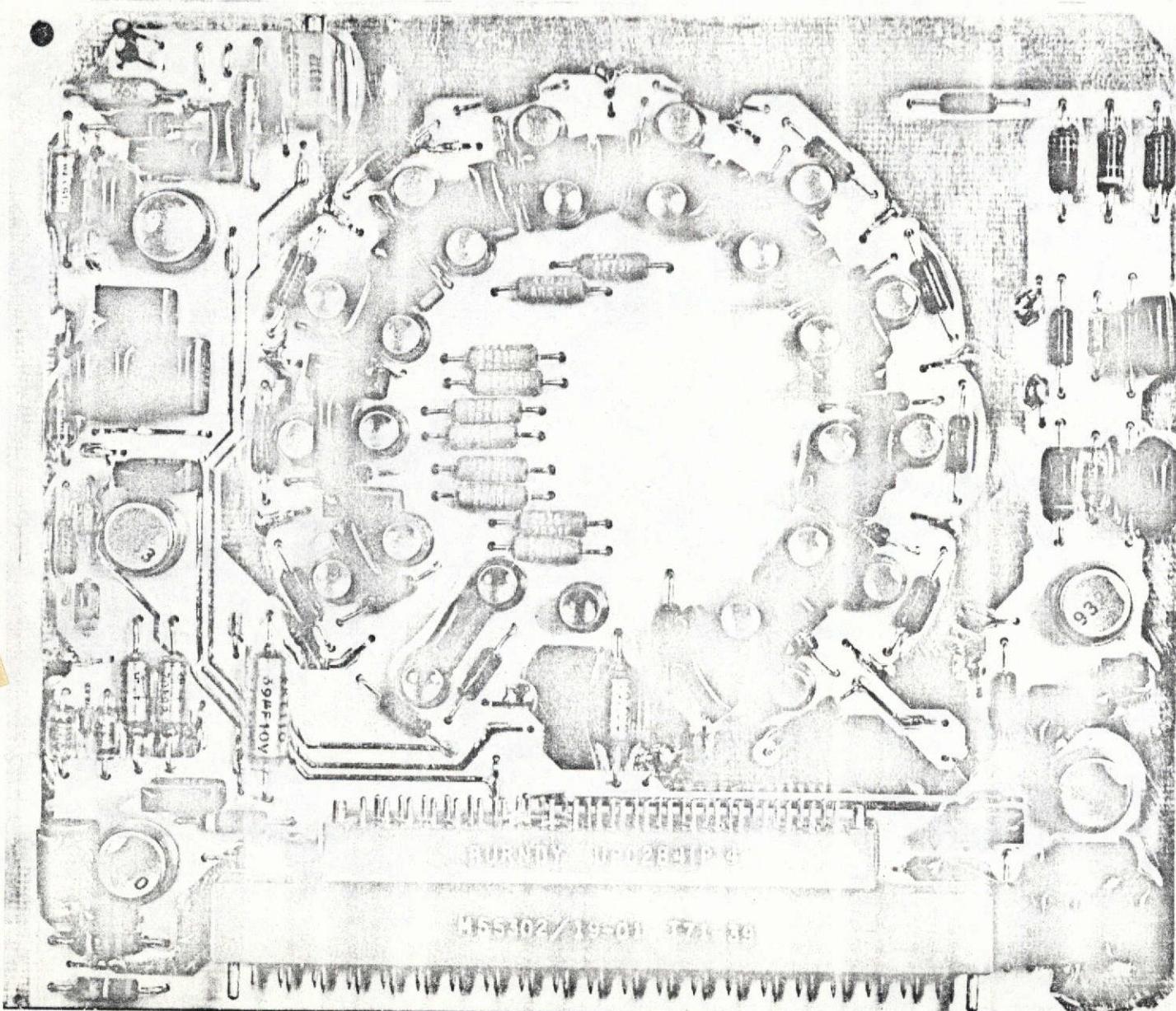
Photograph　　　　　ADC/DAC

Resistors R9, R10 and R11 form a voltage divider to supply a 2.5 volt and 5 volt reference. The 5 volts at the junction of R9 and R10 goes to operational amplifier A3. Amplifier A3 is used as a unity gain buffer amplifier to supply the "Analog Reference Output", which is 5 volts. An overvoltage protection circuit is composed of CR4, CR5, and R14, this protects A3 from voltage accidently applied to Pin 39.

The 2.5 volts at the junction of R10 and R11 connects to the non-inverting input of operational amplifier A2. This amplifier has unity gain at DC and may have greater than or less than unity AC gain with the proper selection of R82 and R96. The nominal value for each resistor is zero. Increasing R82 increases the gain and increasing R96 decreases the gain. Control R88 is fine adjustment of the gain to control the full scale calibration. Emitter follower transistor Q25 is used to boost the current drive capacity of A2.

The DC Analog Circuit operation will be considered next. The +2.5 volt output of Q25 feeds the PNP transistor switches of the ladder network. This 2.5 volt source is used for two reasons: to provide a voltage to turn the PNP transistors on, and a method to obtain the DC analog output from the ladder network. Transistor switches Q1 through Q24 are used in the inverted mode to obtain a very low saturation voltage. Logic signals from the up-down counter control the on or off state of the transistor switches. Assume a logic "1" on the 2048 input. Pin 14 of hex inverter U2 will be low, this will turn Q23 on and Q24 off. This will cause 1/2 full-scale current flow into operational amplifier A4. This inverting amplifier operates with unity gain so therefore, 1.25 volts (1/2 of 2.5 volts) will be the output. The output of A4 goes into A5, an inverting amplifier with a gain of two. Amplifier A5 also opeates as an integrator to remove the AC component of the DC analog signal.

The AC operation will be considered next. The unknown signal from the bridge network (T1) connects to the inverting input of summing amplifier A4 through resistor R67. For a ratio measurement of 20:1, R67 would be increased from 1K ohm to 20K ohm and R87 lowered from infinity to 1050 ohms. The parallel combination of R67 and R87 should equal to 1K ohm.

The reference signal from T2 bridge network connects to the inverting input of A2 through R83 and R96 (R96 should be less than 100 ohms). Amplifier A2 is used as a buffer to drive the R2R ladder network. Since one of each pair of switch transistors is always "on", the current encounters two paths for flow, each of which is exactly 2K ohms. The current, therefore, divides equally with I $1/2$ flowing in R62. At the second mode of the ladder, the current flowing in R61 again sees two equal resistance paths and again splits with I $1/4$ flowing in R58. The current division process continues through the 12 current modes until only increments of I $1/2^{12}$ remains. This increment is discended through R18. The current is therefore separated into 12 binarily weighted parts. From these parts, currents can be selected to yield any fraction of the reference signal from zero to $\frac{4095}{4096}$ with a resolution of $\frac{1}{4096}$. As an example, when 2048 is on (Q23 on) I $1/2$ is flowing through R62 into summing amplifier A4. It contributes a current which opposes the unknown input current. When the proper parts of the reference currents are selected, the sum will cancel the unknown current to give zero output of the summing amplifier A4. The output of A4 is the error signal which goes to the error amplifier and servo-control network where it is used to control the direction of counting of a 12 bit up-down counter. The binary outputs of the counter is in turn used to control the ladder switches.

Therefore, the ladder network balances out the unknown signal in the summing amplifier A4 and also derives the DC analog output from A4.

3.2.4 Filter Error Amplifier

Drawing 2873050 is a schematic of the Filter Error Amplifier. Input stage Q1, T1, C2, and C18 comprise a bandpass filter which is tuned to the frequency of the oscillator. T1 drives a second bandpass filter similar to the first stage filter. It consists of Q2, T2, C5 and C17. The output of T2 goes to the input of U1 a wideband high gain operational amplifier. The output of U1 goes into U2 which is also a wideband high gain amplifier. A control R18, is used to control the gain of the amplifier. Two test signals are provided for use in the DCMS Display Test Set. Error signal low (pin 14) and error signal high (pin 31).

3.2.5 Phase Detector

Drawing 2873035 is a schematic of the bridge phase detector and also includes a built in test equipment circuit (BITE). The BITE monitors the bridge oscillator, the clock oscillator, the power supply, and also indicates when the up-down counter reaches zero count or a count of 4095.

The detector circuit consists of two detector circuits an in-phase and a quadrature detector. The in-phase circuit consists of Q2, Q3, and T1. Transistors Q2 and Q3 are transistor switches which are driven alternately by the balanced drive from the secondary of T1. The signal into the primary of T1 comes from the bridge network and is phase shifted about 90° from the oscillator phase. The error signal input (pin 33) to be detected produces current flow in R22 and R23. The error signal is composed of many frequency components due to noise in addition to the desired signal. It may also have a component of the desired frequency which is 90° out of phase with that which is caused by capacitive unbalance of the bridge. It is desirable for the phase detector to extract from the error signal only the algebraic sign of the desired phase component of the bridge excitation frequency.

NOTES:
UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NUMBER AND ASSEMBLY DESIGNATIONS.
2. REFERENCE DRAWING FOR CIRCUIT CARD ASS'Y D2873052
3. FOR P W BOARD CIRCUIT INTERCONNECT SEE SYSTEM BLOCK DIAGRAM
4. RESISTORS ARE 1/4W, 5% ; DIODES ARE 1N4449.
5. EACH LOGIC SYMBOL REPRESENTS A CIRCUIT FUNCTION WITHIN EACH INTEGRATED CIRCUIT.

Photograph   Filter Error Amplifier

SCHEMATIC, BRIDGE PHASE DETECTOR, DCMS
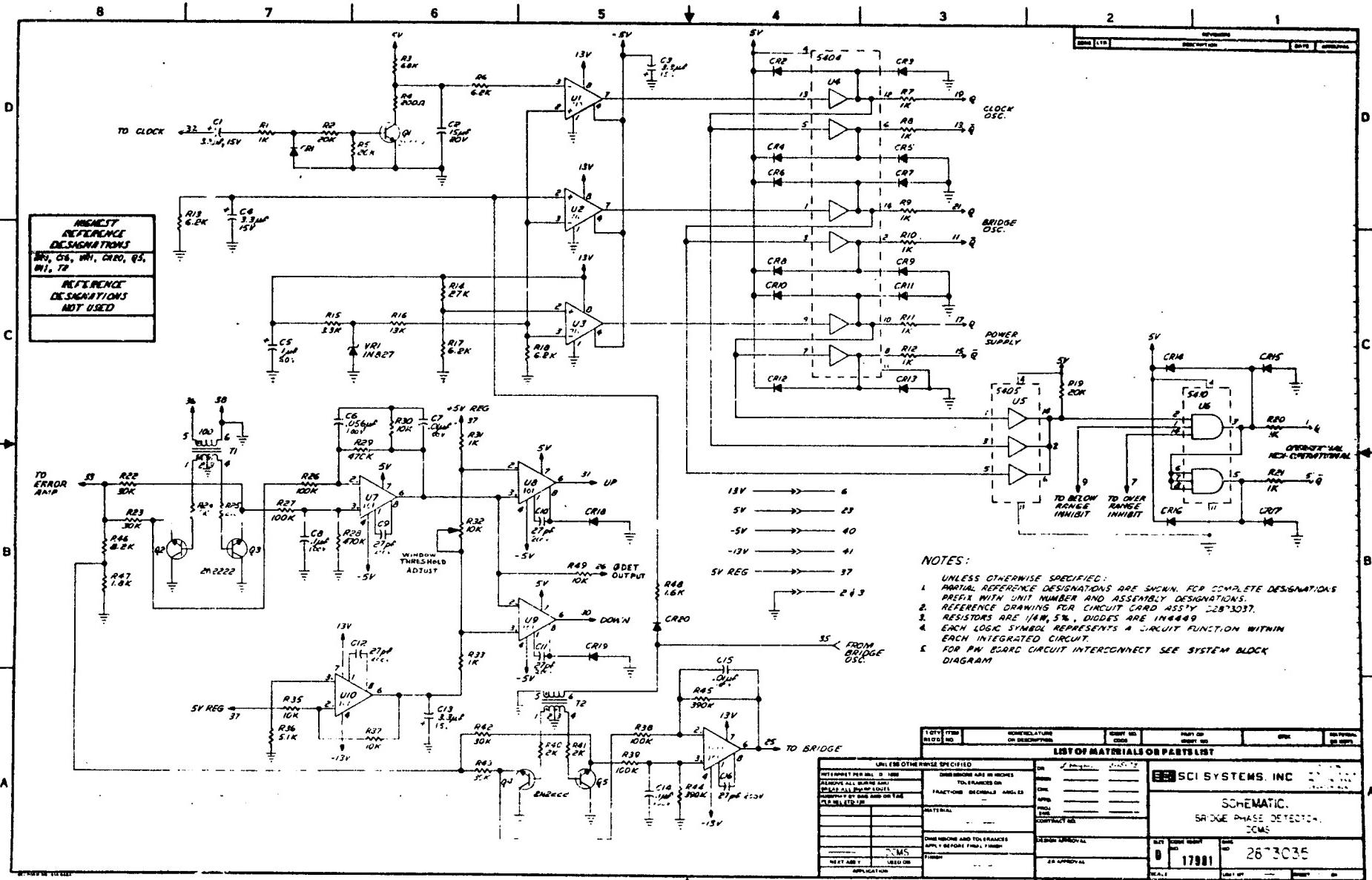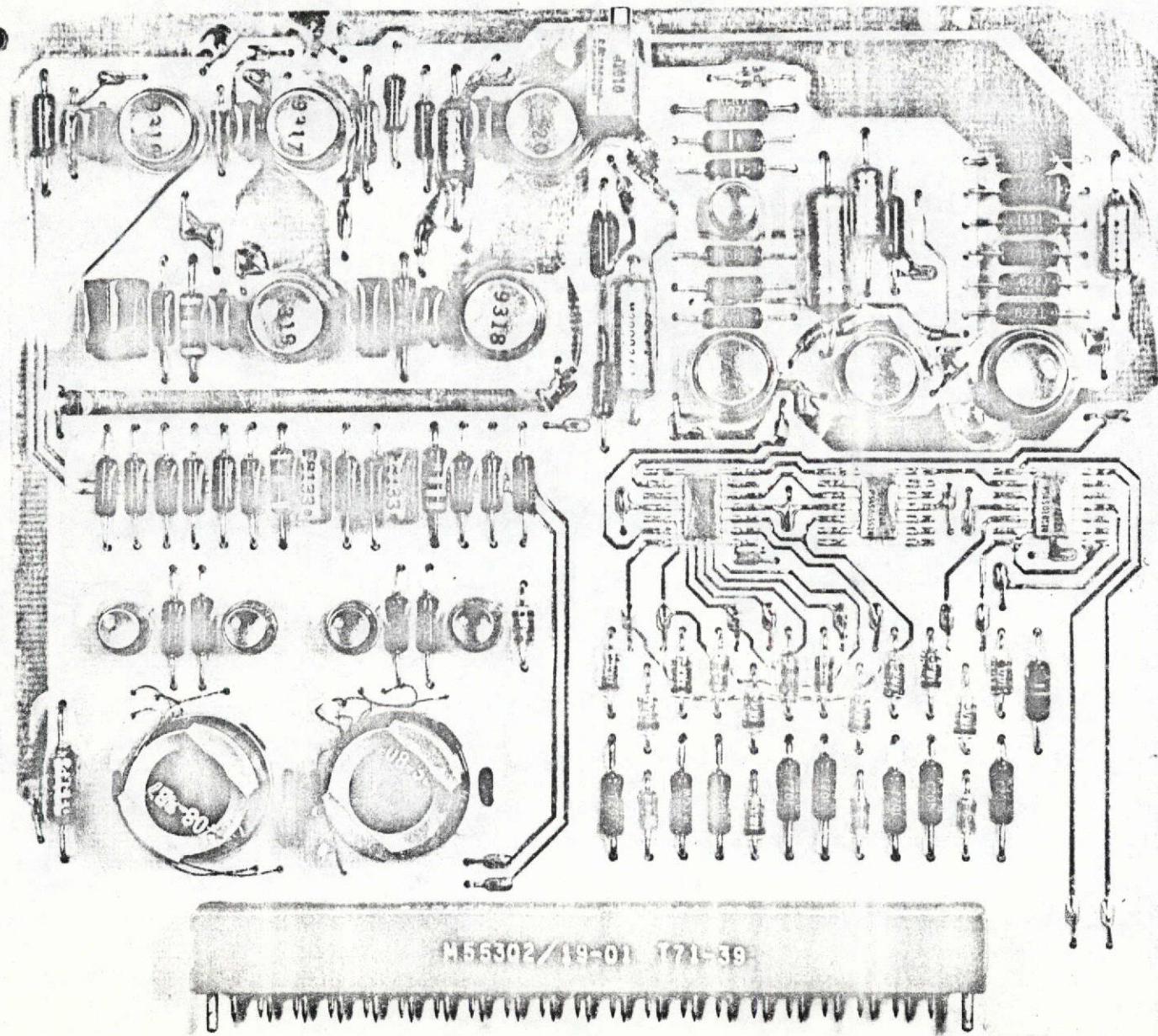
Photograph   Phase Detector

The phase detector does this by effecting a multiplication of the original excitation frequency by the error signal. When Q2 is "on", Q3 is "off" and the current in R22 is integrated in C6. When Q3 is "on", Q2 is "off" and the current thru R23 is integrated in C6 in the opposite direction. Thus, the net current flowing over the second half-cycle is algebraically subtracted from the net current over the first half cycle.

That component of error at the driver frequency can be resolved into in-phase and quadrature components. The in-phase component is of one sign during the first half-cycle and the opposite sign during the second half-cycle so that the net difference over a cycle is the full-wave rectified average of the current. The quadrature component is equally positive and negative over either half-cycle so that the net current is zero over a full cycle.

Components of the error signal which are near the excitation frequency may produce a net current over one complete cycle, but cannot maintain a net current over a number of cycles. A net current integrated over a number of cycles will cause the voltage on C6 to change. Only a component of error which is of the same phase and frequency as the driving voltage will produce a D.C. voltage on C6. The circuit then acts as a very narrow-band filter which is always centered at the bridge excitation frequency and is receptive to only one phase component of that frequency. The D.C. voltage produced on C6 is of like sign of the desired component of error signal. Operational amplifier U7 is used as an integrator with C6. A positive output will cause the up-down counter to count up, and a negative output will cause the counter to count down.

Amplifiers U8 and U9 are used as a window discriminator to decide when to count up, down, or stop counting. A D.C. threshold voltage is provided for

U8 and U9, which is controlled by R32. A +5 volt reference from the ADC is applied to R31 and the inverting input of operational amplifier U10. The output of U10 provides a -5 volt reference to R33. Divider chain R31, R32, and R33 provide a symmetrical ± 4 volts down to zero volts for a threshold voltage to the window discriminator U8 and U9.

As an example, assume that the window threshold potentiometer is set so as to give a ± 1 volt threshold. With the "+" input of U8 at zero volts, and the "-" input at +1 volt the output will be -.6 volt. The outputs of U8 and U9 cannot go to -5V because of diode clamps CR18 and CR19, but are limited to about -.6 volt. Also with zero volts on the "-" input of U9 and -1 volt on the "+" input, the output of U9 will be -.6 volt. Therefore both U8 and U9 outputs are low and the counter cannot count unless one of these outputs is high. If the "+" input to U8 rises to greater than +1 volt the output of U8 will go high to about +4 volts. There is no change in the output of U9. Therefore with U8 high and U9 output low, the counter will count up. If the "-" input to U9 goes to -1 volt the output of U9 will be high and the output of U8 low. This means that the counter will count down.

So if there is about 1 volt peak-to-peak noise on the phase detector output of U7, the window threshold should be set to slightly greater than ± 1 volt to eliminate the noise jitter to the up-down counter. This also keeps the counter from counting up 1 bit, down 1 bit, up 1 bit, etc., at a time when there is no change in the probe capacitance.

The error signal is also applied to the quadrature phase detector transistors Q4 and Q5 thru resistor divider R46 and R47. This detector functions just like the in-phase detector except it detects the quadrature component of the error signal. Transistor switches Q4 and Q5 are driven alternately by the

balanced drive from the secondary of T2. The drive into T2 is about 17 volts peak-to-peak and is the same phase as the oscillator. Operational amplifier U11 is the integrator and its output goes to the FET's on the bridge board to provide automatic nulling of the quadrature component of the error amplifier.

Transistor Q1 and comparator amplifier U1 are part of the BITE. If the clock oscillator should fail, transistor Q1 would turn off allowing capacitor C2 to charge in a positive direction. A +2 volt threshold is applied to the inputs of U1, U2, and U3. This is derived from reference zener diode VR1, and resistor divider R16 and R18. As C2 charges positive it will cause the output of U1 to go to a "0" output from a "1" output state. This will cause U4 clock oscillator Q output pin 19 to go to a "1" output indicating a failure. U4 output 1C pin 12 also drives an inverter for the $\overline{Q}$ output and U5 pin 3. A failure turns U5 input from a "0" to a "1", this places a "0" on the input of U6, which causes "1" (failed) output on the Q output of the "operational non-operational" output pin 1.

The oscillator test circuit functions in a similar way. Diode CR20 half-wave detects the bridge oscillator signal and is applied to U2 input with voltage divider R48 and R13. Capacitor C4 is used to remove the ripple from the oscillator rectification process. If the bridge oscillator fails, the voltage on C4 will drop below 2 volts and cause the output of U2 to change from a "1" output to a "0" output state. The inverter and gate circuit function just like the clock oscillator circuit.

Comparatro U3 monitors the power supply output voltage. If the supply voltage drops enough for the +input of U3 to go below about 2 volts, the output of U3 will change from a "1" output to a "0" output. This will indicate a problem with the power supply when the "power supply" Q output changes from a "0" output to a "1" output. The inverter and gate circuit functions the same as the clock oscillator circuit.

3.2.6   Up-down Counter

The up-down counter is divided between two printed circuit boards. The
counter circuit is shown on two schematic drawings 2873047 and 2873038.
Drawing 2873047 will be discussed first. The clock oscillator consists of
C3, R3, R4, R5, and three inverters of U7. The three inverters provide the
gain and positive feedback necessary for a free running oscillator. The free
running frequency is about 100 KHz and determined by R3, R4, and C3. A
sync amplifier U9 receives a TTL signal on its input and synchronizes the
oscillator thru one of the inverters. Amplifier U10 receives a TTL inhibit
signal and is used to inhibit the clock oscillator thru one of the inverters.
The output of the last inverter of U7 is coupled to 1/3 of U8 and both are
used as buffer amplifiers for the clock output. The clock squarewave is
AC coupled and differentiated into the two 3-input gates U8. Resistor R15
holds two of the gate inputs low, so both gate outputs will be high. The
leading edge rise time of the clock would cause both gate outputs to go
netative to a low and produce a narrow width pulse. However, both gate
outputs must not be allowed to produce negative pulses at the same time.
The up or down count command signals from the phase detector enter into
gate U8 on pins 2 and 6 respecitvely. The count commands will both be
low to stop counting and a high signal will cause that particular command to
count up or down. For example if the up command goes high the counter
should count up. With a command to count up the down command will be low,
this will keep pin 5 of U8 high during the clock pulse. This will allow the
counter U3 to count up. Two additional signals are connected to the gate
inputs, zero inhibit and full inhibit. A zero inhibit signal is produced when
all 12 counter outputs are low. This provides a low on pin 7 of gate U8,
which inhibits the output of U8 and will not allow the counter to count down.
The same thing happens when all 12 of the counter outputs go high, a low is
provided on pin 1 of gate U8 and will not allow the counter to count up. The
zero inhibit is generated by open collector hex inverters U5 and also U2 on
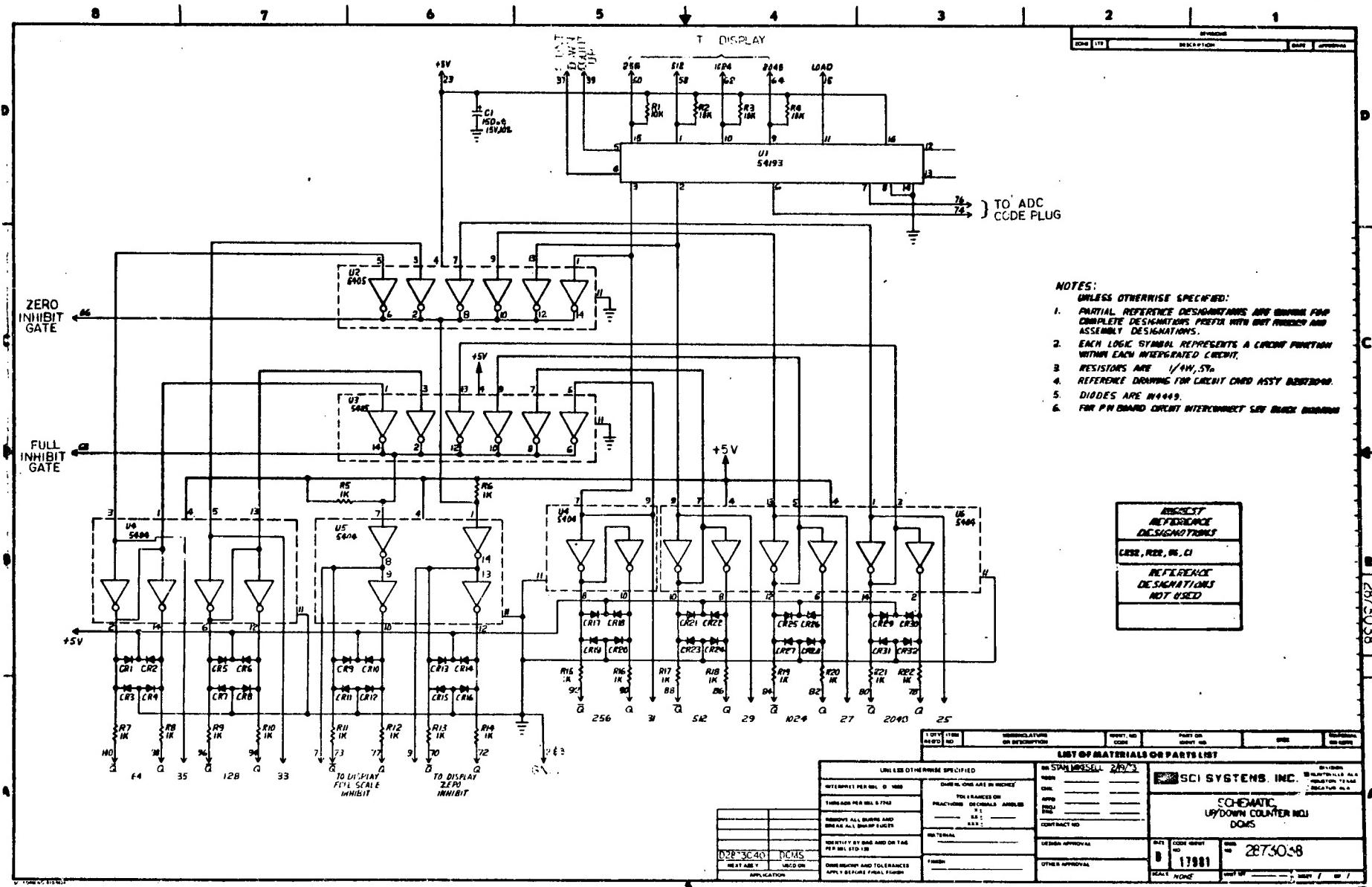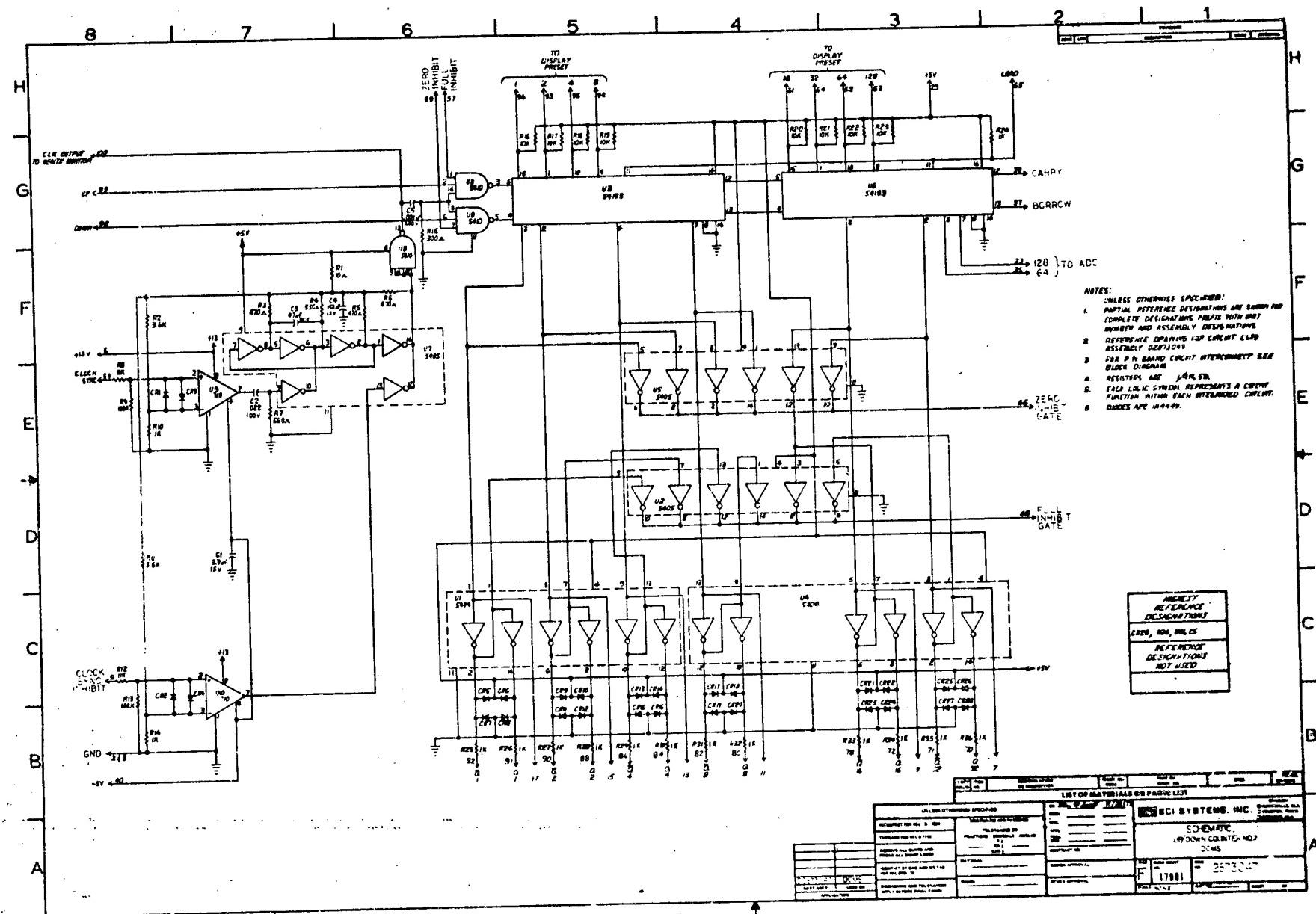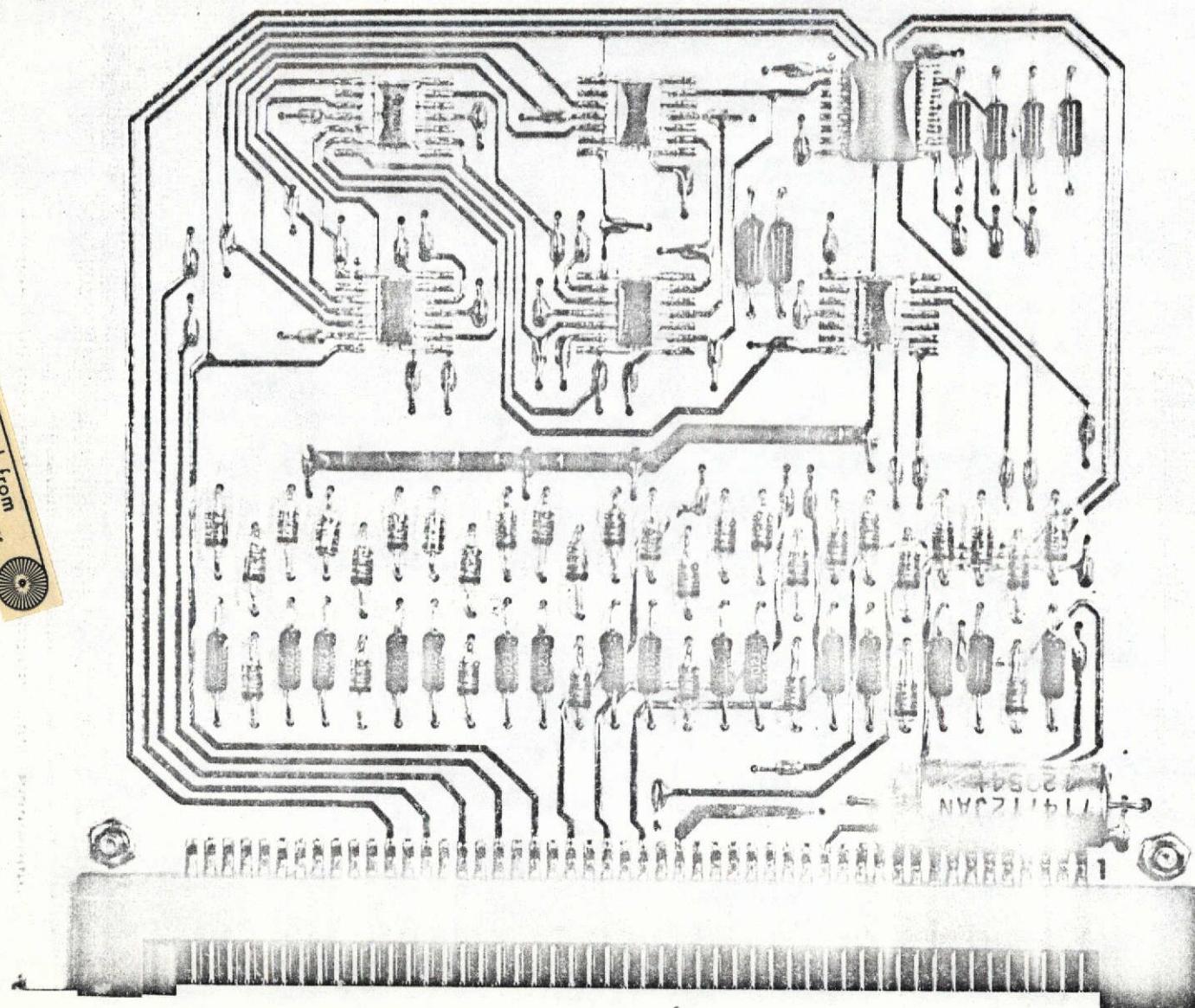
SCHEMATIC,
UP/DOWN COUNTER NO.1
DCMS

2873038

Photograph   Up-Down Counter No. 1

Photograph   Up-Down Counter No. 2

Point Sensor No. 2

Point Sensor No. 1

Oscillator

Bridge Network

Phase Detector

Filter Error Amplifier

ADC/DAC

Up-Down Counter No. 2

Up-Down Counter No. 1

Power Supply
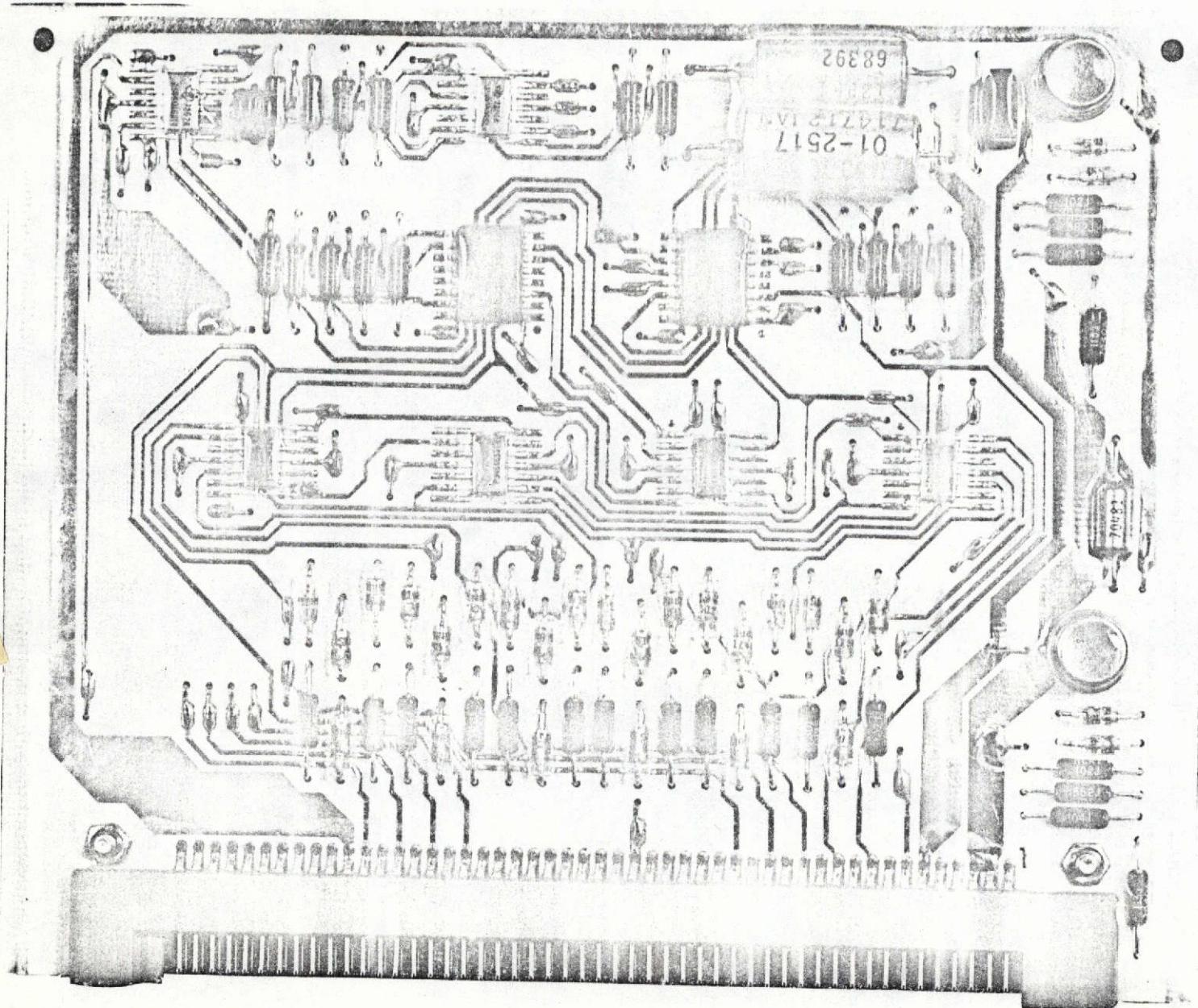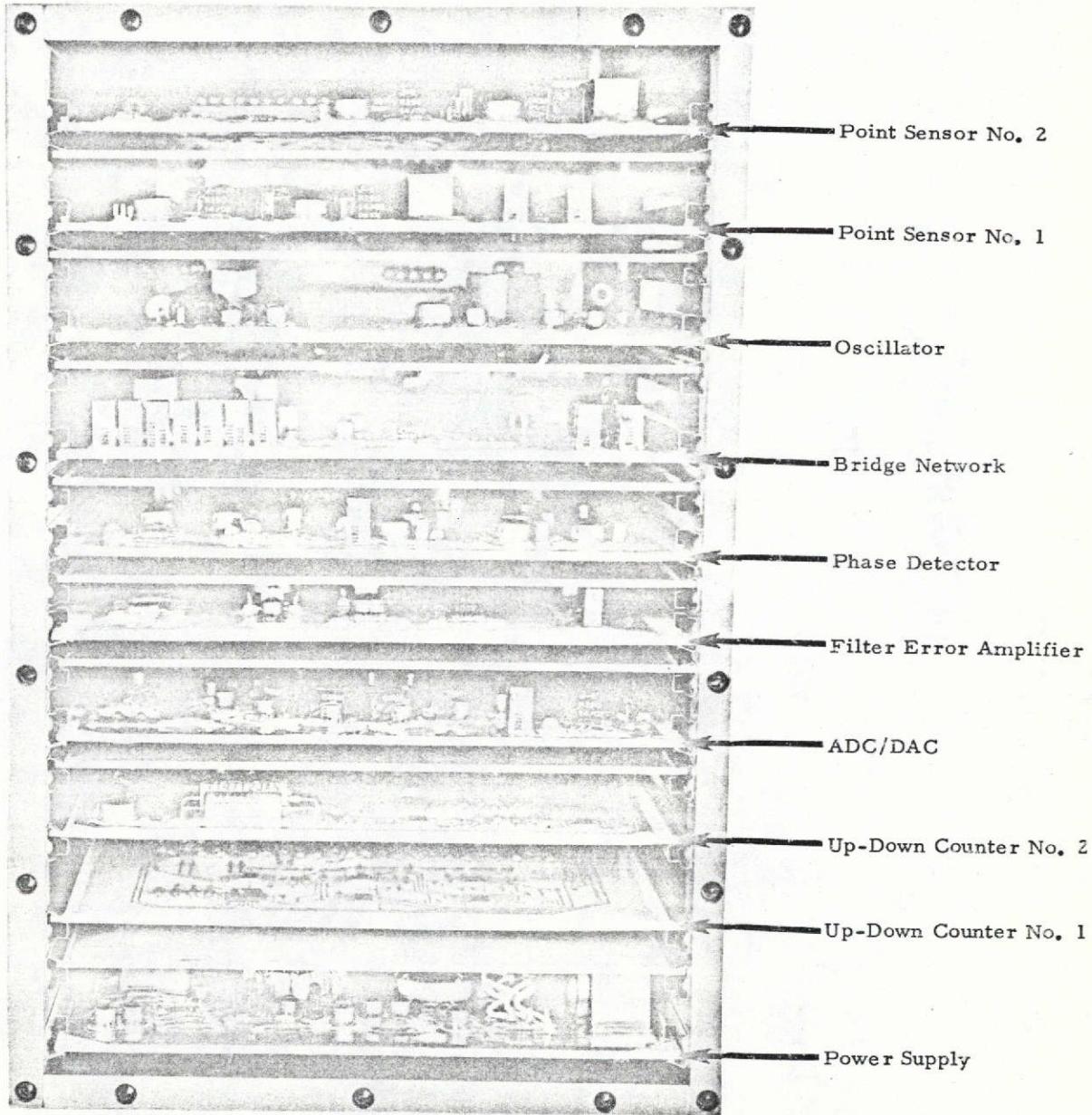
DCMS PW Board Location

schematic 2873038. The full scale inhibit is generated by open collector hex inverter U2 and also U3 on schematic 2873038.

The 12 bit counter consists of U3, U6, and also U1 on schematic 2873038. In addition to being capable of counting up or down, each output may be preset manually with twelve switches on the DCMS Display Unit.

Each counter output and the two inhibit signals are buffered and inverter to provide both Q and $\overline{Q}$ outputs. This is provided by 5 hex inverters, U1 and U4 on schematic 2873047 and U4, U5, and U6 on schematic 2873038. The hex inverter outputs are protected from $\pm$ over-voltages which might be inadvertently applied, this consists of a resistor and 2 diodes for each output. For example R25, CR5, and CR7 of U1.

3.2.7   Point Sensors

The point sensor circuit is shown on schematic drawings 2873041 and sheet 1 and 2 of drawing 2873044. The point sensor circuitry is designed to signal condition 6 discrete liquid level probes of 5 pF each nominal capacitance when empty.

Figure 3 shows a simplified drawing of point sensor No. 1 and some circuitry common to all point sensors. The point sensor probe P_C causes a current flow from the main probe E+ voltage into the point sensor transformer T1 and is of a phase.to oppose the current from probe P_C. This reference voltage is provided by transformer winding on the oscillator printed circuit board. Each tapped section of the transformer provides about 2.5 volt peak-to-peak for a total of about 7.5 volts peak-to-peak. The normal operating voltage to the reference capacitor C3 is adjustable from about 2.5 to 5 volts peak-to-peak with calibrate potentiometer R8.
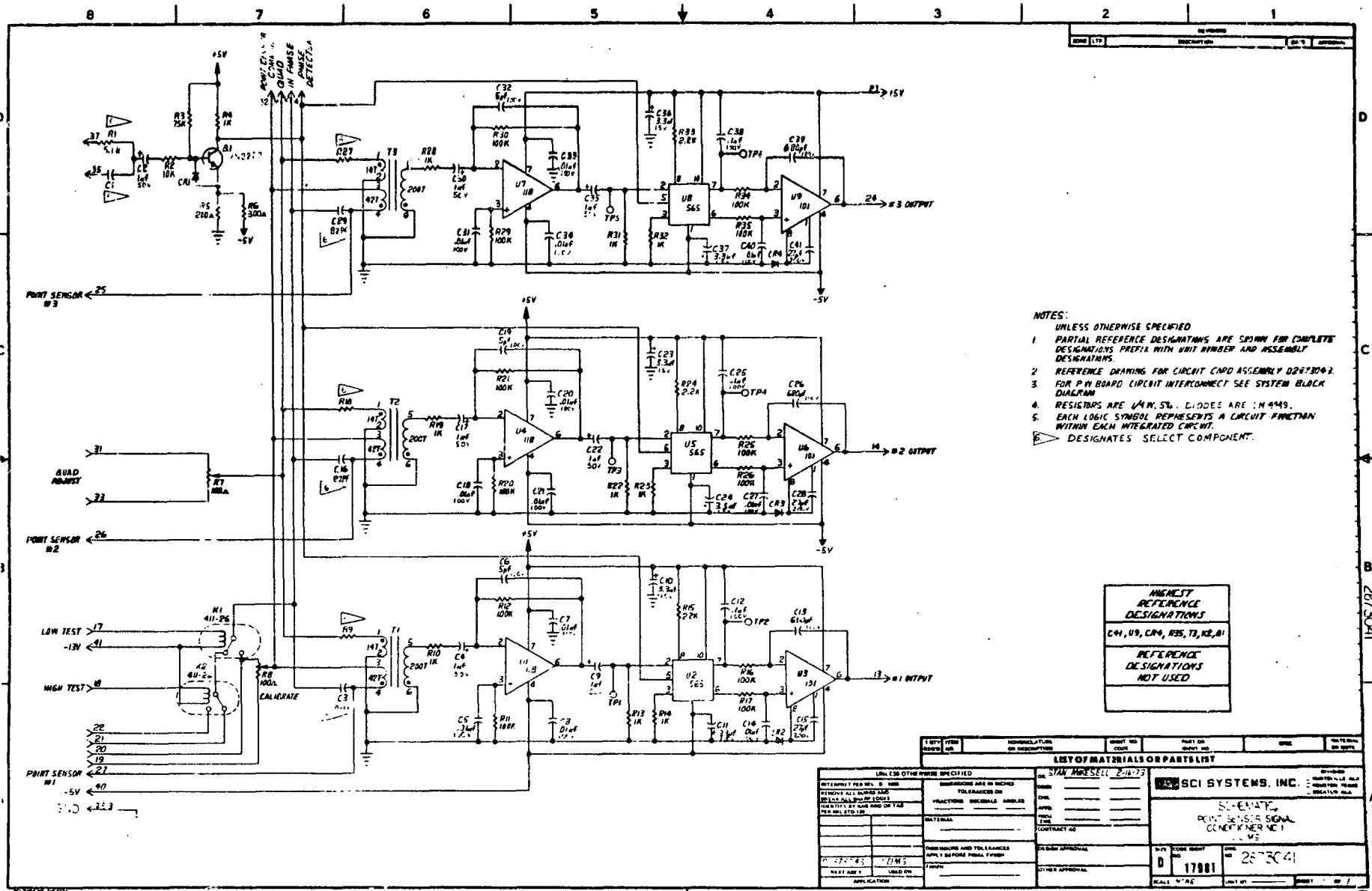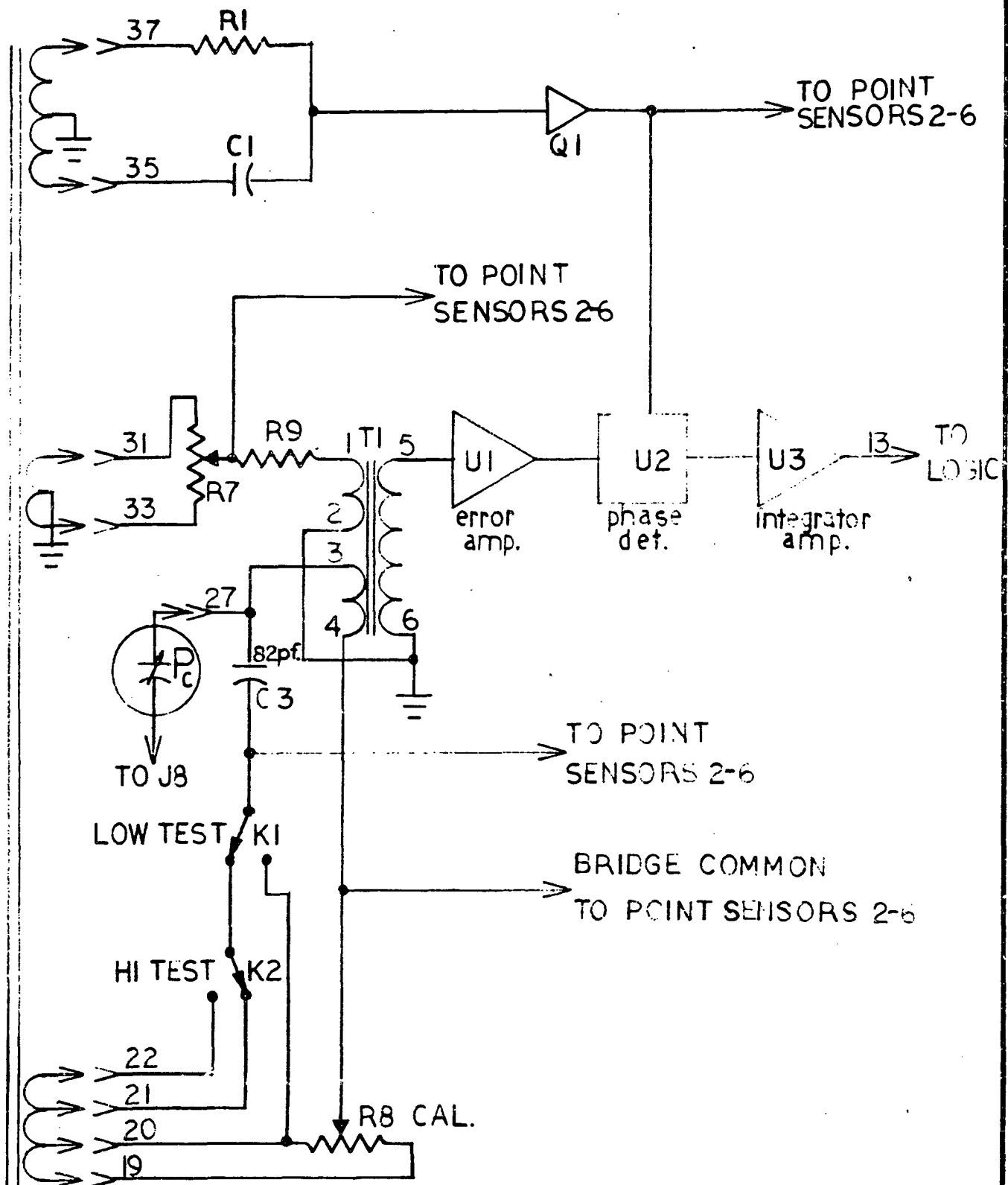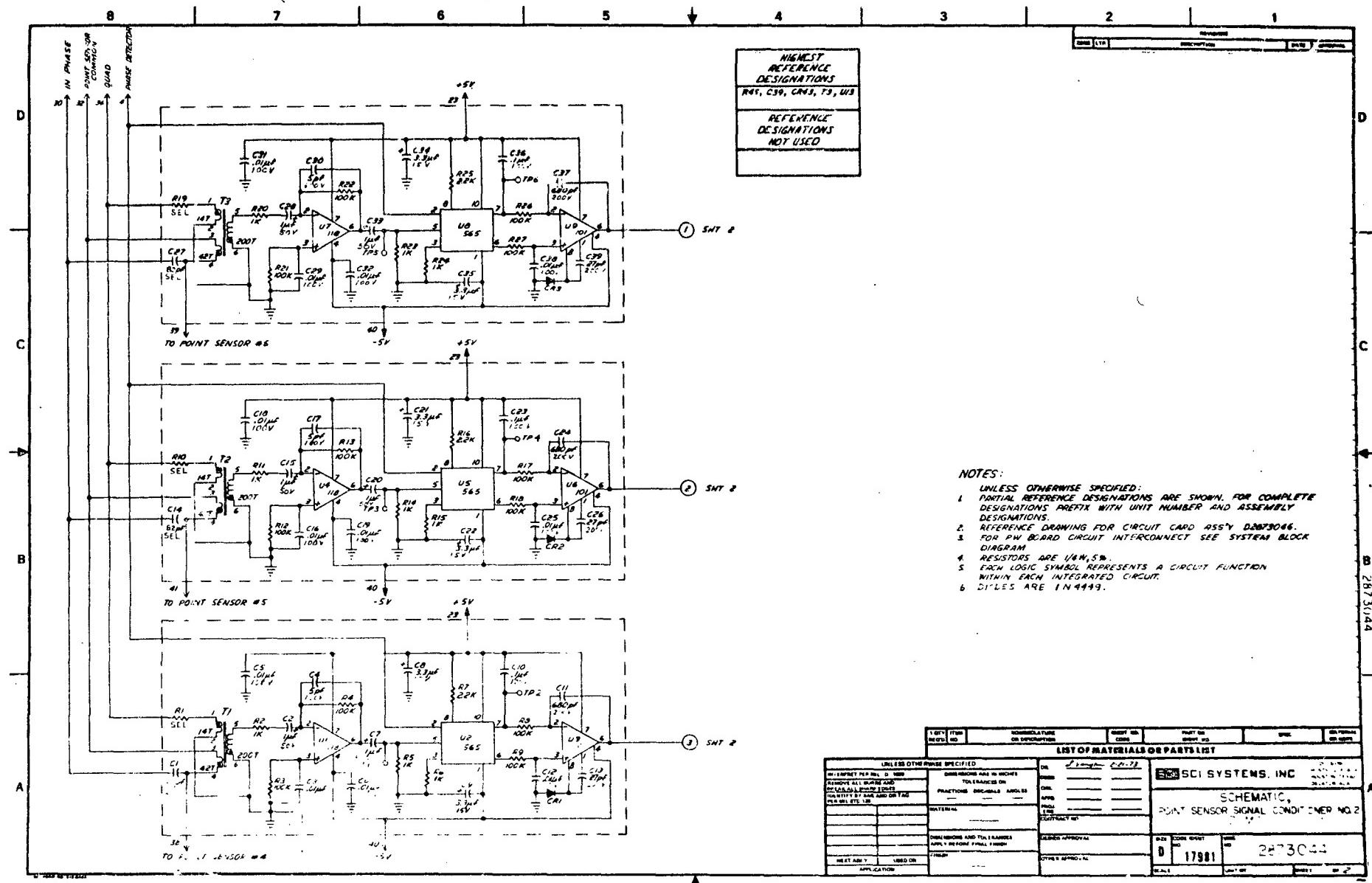
SCHEMATIC
POINT SENSOR SIGNAL
CONDITIONER NO 1

SCI SYSTEMS, INC.

NOTES:
UNLESS OTHERWISE SPECIFIED
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NUMBER AND ASSEMBLY DESIGNATIONS.
2. REFERENCE DRAWING FOR CIRCUIT CARD ASSEMBLY D2873043.
3. FOR P/W BOARD CIRCUIT INTERCONNECT SEE SYSTEM BLOCK DIAGRAM
4. RESISTORS ARE 1/4 W, 5%. DIODES ARE 1N4449.
5. EACH LOGIC SYMBOL REPRESENTS A CIRCUIT FUNCTION WITHIN EACH INTEGRATED CIRCUIT.
6. DESIGNATES SELECT COMPONENT.

FIGURE 3

CODE IDENT NO 17981 | DWG SIZE A | OF | REV

SCI FORM NO. 810-052 (Rev. 6/18/73)

Schematic, Point Sensor Signal Conditioner No. 2

NOTES:
UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NUMBER AND ASSEMBLY DESIGNATIONS.
2. REFERENCE DRAWING FOR CIRCUIT CARD ASS'Y D2873046.
3. FOR PW BOARD CIRCUIT INTERCONNECT SEE SYSTEM BLOCK DIAGRAM
4. RESISTORS ARE 1/4 W, 5%.
5. EACH LOGIC SYMBOL REPRESENTS A CIRCUIT FUNCTION WITHIN EACH INTEGRATED CIRCUIT.
6. DIODES ARE 1N4449.

THREE BIT WORD

POINT SENSOR OUTPUTS

2873044

Labels on board: TP6, TP5, TP4, TP3, TP2, TP1

M55302/19-01   171-39

Photograph   Point Sensor No. 1

Photograph   Point Sensor No. 2

Relay K1 is used to test a low probe (empty). The current from the reference capacitor C3 is larger than the current from probe P_C. When relay K1 is energized it reduces the voltage 2.5 volts to C3 and then the current from the probe will be greater and cause the output of U3 to indicate a full probe.

Relay K2 is used to test a full probe. The current from the full probe P_C is larger than the current from the reference capacitor C3. When the high test relay K2 is energized, it increases the voltage to C3 2.5 volts and therefore the current due to the reference capacitor C3 will be greater. This will cause the output of U3 to change from a full probe indication to an empty probe state.

Potentiometer R7 is a quadrature null adjustment to null the quadrature of all the probes simultaneously.

The output of transformer T1 goes into a wideband high gain operational amplifier U2 which is used as an error amplifier. The output of U1 goes into the phase detector U2. Resistor R1 and capacitor C1 provide a 90° phase shift for the phase detectors. A 17 volt peak-to-peak sine wave from the oscillator is applied to R1 and 180° phase difference to C1. This 90° shifted sine wave is limited and squared in amplifier Q1. Therefore Q1 provides a 90° phase shifted square wave to each point sensor phase detector.

The output of phase detector U2 goes to the input of U3, an operational amplifier used as an integrator. This removes the AC component and provides high DC gain to increase the signal level of the phase detector output.

Schematic 2873041 and sheet 1 of 2873044 show the six point sensor circuitry which produces 6 discrete outputs. Sheet 2 of 2873044 shows the logic to buffer the 6 discrete outputs and generates a 3 bit word.

Hex inverters U12 and U13 are used as buffers and inverters for both Q and $\overline{Q}$ outputs of the 6 point sensor outputs. A triple 3-input gate is used to generate the three-bit word. An inverter is used to produce $\overline{Q}$ for each output of the 3-bit word. A 1K ohm resistor and 2 diodes are used on each output for protection of an over voltage which might be applied to an output accidently.

3.2.8 Power Supply

Schematic drawing number 2873029 shows the power converter. The part of this system which is most critical to the operation of the unit and determines its ability to meet the regulation and EMI requirements is the regulator arrangement. This cannot, in general, be a simple series regulator since the power dissipation which is incurred at nominal input voltage, if it is set up to operate correctly at the minimum voltage, is prohibitive both from a total efficiency point of view and due to the thermal aspects of the concentration of high dissipation in one area.

The regulator which is used is a synchronized PDM stepdown pre-regulator in which the series element Q10 is operated in a switching mode. The duration of the on period pulses fixes the mean output voltage from the regulator and the square waves are LC integrated by L3 and C9-C10 to provide dc to the square wave dc/dc converter.

The operation is as follows. The leading edge of the dc/dc converter square wave is differentiated to provide a synchronizing pulse to lock the frequency of the regulator to that of the converter.
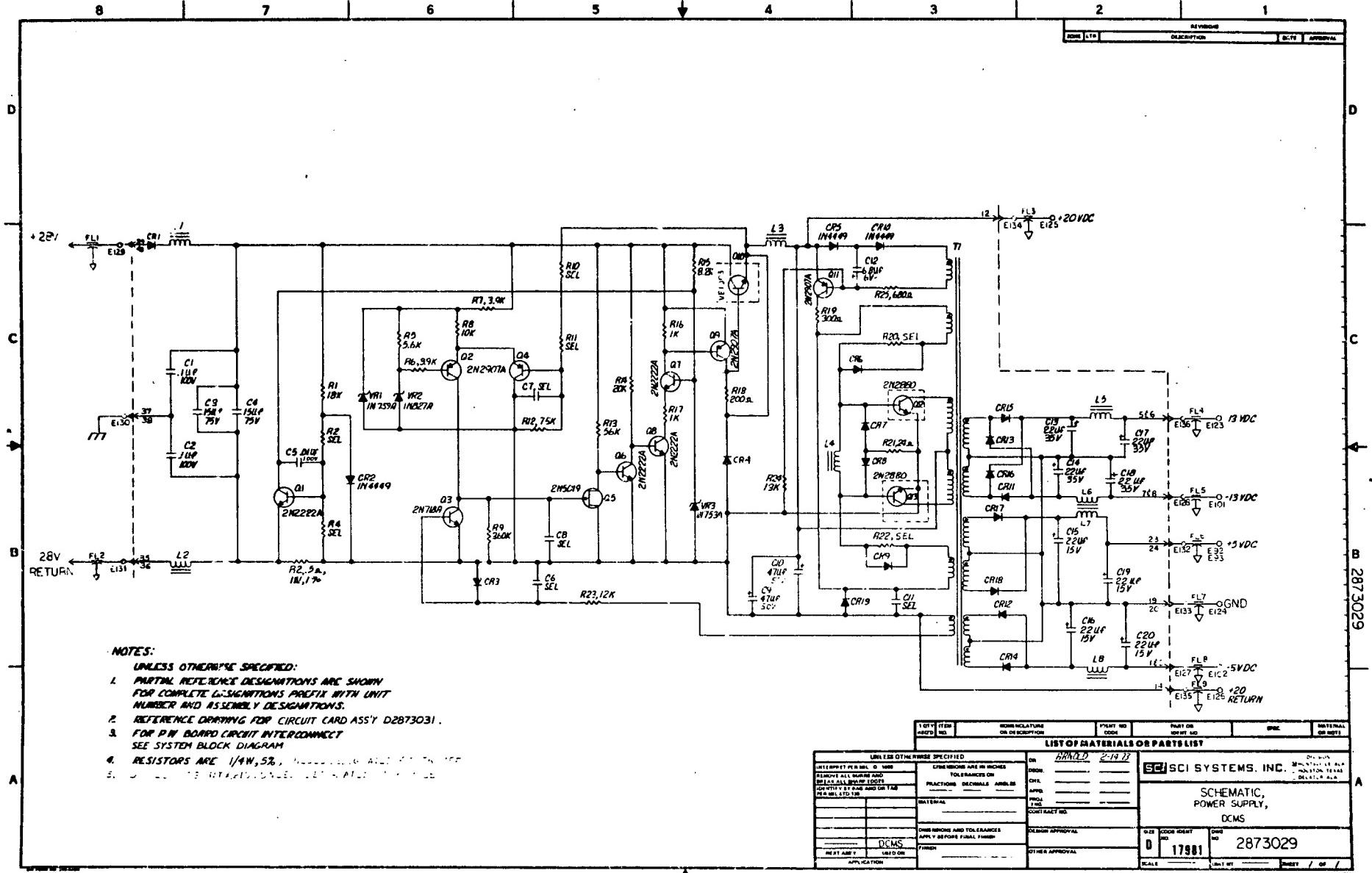
SCHEMATIC,
POWER SUPPLY,
DCMS

NOTES:
UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATIONS PREFIX WITH UNIT NUMBER AND ASSEMBLY DESIGNATIONS.
2. REFERENCE DRAWING FOR CIRCUIT CARD ASS'Y D2873031.
3. FOR P/W BOARD CIRCUIT INTERCONNECT SEE SYSTEM BLOCK DIAGRAM
4. RESISTORS ARE 1/4W, 5%,

CODE IDENT NO.	DWG NO.
D 17981	2873029
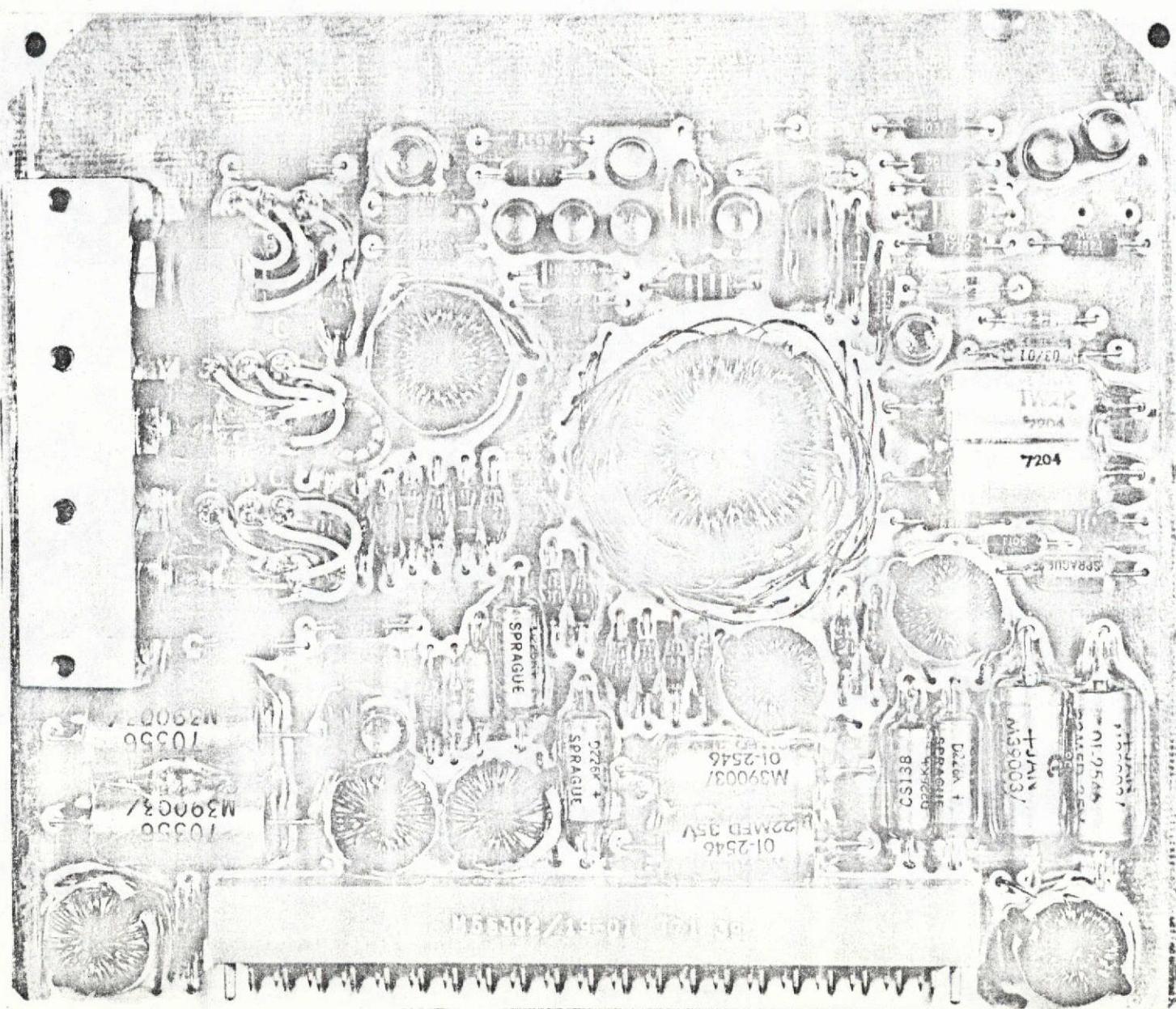
Photograph   Power Supply

The sync pulse turns on a transistor Q5 which rapidly discharges the regulator timing capacitor C8. C8 is contained within the feedback loop of a series regulator type amplifier so that when C8 is discharged to ground, the series transistor Q10 is switched off. At the end of the short sync pulse, C8 is charged linearly by the differential input amplifier Q2-Q1 until a voltage is reached which brings the series transistor back on. The feedback action adjusts the balance of the differential amplifier so that the charging current to C8 and hence, the switch period duration, is modulated to maintain the feedback voltage equal to a fixed reference.

Some features of this arrangement are that under start-up conditions the circuit reverts to a series regulator and power is provided to start the converter even under low voltage conditions. Also, under over-voltage and surge conditions, the high voltage is developed only across the series switch and driver and the regulator continues to provide the regulated output to the convert. Additionally, the circuit is by nature a low pass filter and thus gives good rejection of ac ripple imposed on the dc input lines. This rejection is improved by the LC filter which is in the input leads for EMI suppression reasons. Reverse polarity protection is also included on the input line by CR1.

The dc/dc converter which the pre-regulator supplies is a single transformer circuit running at approximately 125 KHz in which the drive to the converter switches is obtained from positive feedback windings on the power transformer. The power transformer is not allowed to saturate due to the presence of a timing inductor L4 on the converter switch base drive. A very small square loop inductor L4 is used to dump base current when it saturates after a fixed time interval. The regenerative switch cycle is thus made to occur without the large current spikes which characterizes the standard converters of this type.

An additional feature is the switch start-up circuit which provides adequate start-up current for any voltage and temperature combination and is automatically biased off when the oscillator starts to conserve that current and improve efficiency. This start-up current is provided by Q11.

These features are combined to provide an efficient pre-regulated converter which has been proven by experience. Typical all conditions output stability of 5% and an high overall efficiency are obtained.

The output voltages of T1 are rectified and filtered and then must pass thru RFI filters for very low RFI output.

4.0   SPECIFICATION

4.1.0   SCOPE

This specification covers the electrical performance of the Digital Capacitance Measuring System to be used with the shuttle propellant management systems and ground support equipment.

4.1.1   CLASSIFICATION

The Digital Capacitance Measuring System, referred to as the DCMS unit, provides maximum flexibility for accommodating various modes of operation, operating ranges and sync capabilities. The system consists of a continuous capacitance measuring system and a discrete capacitance system capable of monitoring six (6) point sensor probes.

4.2.0   REQUIREMENTS

4.2.1   PERFORMANCE

4.2.1.1   Functional Characteristics

The DCMS is capable of continuous capacitance measurement in one of three modes of operation: 1) Absolute Capacitance, 2) Capacitance Ratio, and 3) Capacitance difference. The DCMS also provides for six discrete capacitance measurements which can be used in conjunction with the continuous system in order to expand its resolution or indepdently.

4.2.1.1.1   Continuous Capacitance Measurement

4.2.1.1.1.1   Operating Modes

    a.   Absolute Capacitance

    b.   Capacitance ratio

    c.   Capacitance difference

4.2.1.1.1.2   Operating Range and Sensitivity

   a.   Absolute Capacitance
         Range: 5 pf to 1000 pf full scale
         Sensitivity: 5/1024 pf for 10 bit system
                       5/4096 pf for 12 bit system

   b.   Capacitance Ratio
         Range: Reference capacitor 5 pf to 1000 pf,
                 Capacitance ratio 200:1 full scale maximum
                 with 5 pf reference capacitor, capacitance
                 ratio of 1:1 full scale maximum with 1000 pf
                 reference capacitor.
         Sensitivity: 5/1024 x ratio for 10 bit system
                       5/4096 x ratio for 12 bit system

   c.   Capacitance Difference
         Range: Common Mode and Difference
                       5 pf and   1000 pf
         Sensitivity: 5/1024 for 10 bit system
                       5/4096 for 12 bit system

4.2.1.1.1.3   Accuracy: $\pm$ .075% $\pm$0.1 pf x capacitance ratio.

4.2.1.1.1.4   Bridge

4.2.1.1.1.4.1   Excitation Frequency: 30 kHz to 90 kHz

4.2.1.1.1.4.2   Excitation Voltage: 50 volts peak to peak nominal with
                     5% differntial adjustment.

4.2.1.1.1.4.3   Output Impedance: 50 ohms nominal for absolute and
ratio operating modes and 75 ohms
nominal for difference mode

4.2.1.1.1.4.4   Input Impedance: 5, 20, or 45 ohm top

4.2.1.1.1.5   Counter Clock

4.2.1.1.1.5.1   Frequency: Nominal 100 Hz free-running, 10 kHz
maximum external sync for 10 bit system,
2.5 kHz for 12 bit system

4.2.1.1.1.5.2   Sample Command: a clock inhibit is provided for
data sample hold.

4.2.1.1.1.7   Cable Length: A maximum of 92 meters of co-axial
cable with capacitance of 30 pf per foot.

4.2.1.1.2   Discrete Capacitance Measurement (Point Sensor)

4.2.1.1.2.1   Operating Range and Sensitivity
Range: 5 pf to 50 pf for 6 measurement operation or
5 pf to 300 pf for single measurement
Sensitivity: .1%

4.2.1.1.2.2   Accuracy $\pm$ 1%

4.2.1.1.2.3   Bridge

4.2.1.1.2.3.1   Excitation Frequency: Same as continuous measurement
bridge.

4.2.1.1.2.3.2   Excitation Voltage: 50 volts peak to peak nominal

4.2.1.1.3   Power Converter

The DCMS power converter operates from a dc power bus of 28 $\pm$ 15% VDC.
The DCMS unit draws a maximum of 0.8 amperes from the 28 volts bus.

4.2.1.1.4   Interface Requirements

4.2.1.1.4.1   Digital Outputs

4.2.1.1.4.1.1   Continuous Capacitance Measurement:
                      10 or 12 bit binary word present for parallel transfer.

4.2.1.1.4.1.2   Discrete Capacitance Measurement
            a)   3 bit binary word representing sequential trip of the
                      six measurements
            b)   A single bit for each of the six measurements representing
                      their status

4.2.1.1.4.1.3   BITE
            a)   A single bit for each of the three test points and for
                      over-range and under-range indication
            b)   A single bit representing the cummulative status of the
                      tests points and the range indicators. (Operate/Non-
                      Operate).

4.2.1.1.4.2   · Analog Output: An analog conversion of the digital output
                      of the continuous capacitance measurement
                      is provided.

4.2.1.1.4.3   Interface Definition
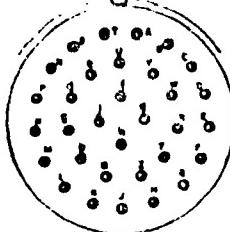
CONNECTOR FUNCTION ~~ПАР~~
TEST SET INTERFACE

TITLE: 2873-545-104

MODEL: DCMS

REVISION: A

CONNECTOR: J1 AFD54-18-32SN

PIN NO.	A to J5A/E117
FUNCTION:	Below Range Inh Q
VOLTAGE:	0V to 0.4V/
	2.4V to 5.5V DC
ORIGIN:	Up/Down Counter
DESTINATION:	Test Set
SOURCE Z:	
LOAD Z:	≥ 10 K ohms

PIN NO.	E to J5G/E51
FUNCTION:	Health Mon-Power Supply
VOLTAGE:	0V to 0.4V/
	2.4V to 5.5V DC
ORIGIN:	Health Monitor
DESTINATION:	Test Set
SOURCE Z:	
LOAD Z:	≥ 10 K ohms

PIN NO.	B to J5C/E115
FUNCTION:	Over range Inh. Q
VOLTAGE:	0V to 0.4V/
	2.4V to 5.5V DC
ORIGIN:	Up/Down Counter
DESTINATION:	Test Set
SOURCE Z:	
LOAD Z:	≥ 10 K ohms

PIN NO.	F to J5J/E49.
FUNCTION:	Health Mon-Bridge OSC.
VOLTAGE:	0V to 0.4V/
	2.4V to 5.5V DC
ORIGIN:	Health Monitor
DESTINATION:	Test Set
SOURCE Z:	
LOAD Z:	≥ 10 K ohms

PIN NO.	C
FUNCTION:	
VOLTAGE:	
ORIGIN:	
DESTINATION:	
SOURCE Z:	
LOAD Z:	

PIN NO.	G to J5L/E50
FUNCTION:	Health Mon-Clock
VOLTAGE:	0V to 0.4V/
	2.4V to 5.5V DC
ORIGIN:	Health Monitor
DESTINATION:	Test Set
SOURCE Z:	
LOAD Z:	≥ 10 K ohms

PIN NO.	D to E99
FUNCTION:	Clock Sync Input
VOLTAGE:	0V to 0.4V/
	2.4V to 5.5V DC
ORIGIN:	External Source
DESTINATION:	Test Set
SOURCE Z:	2 K ohms
LOAD Z:	≤ 180 ohms

PIN NO.	H to J4A/E19
FUNCTION:	3 Bit Word 1 Q
VOLTAGE:	0V to 0.4V/
	2.4V to 5.5V DC
ORIGIN:	Point Sensor
DESTINATION:	Test Set
SOURCE Z:	
LOAD Z:	≥ 10 K ohms

CONNECTOR FUNCTION
TEST SET INTERFACE

PIN NO.   J to   J4C/E21
FUNCTION: 3 Bit Word 2 Q
VOLTAGE: 0V to 0.4V/
            2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: Test Set
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   N to   J3d/E62
FUNCTION: ADC/DAC Ref. Out
VOLTAGE: 5 V DC

ORIGIN: ADC/DAC
DESTINATION: Test Set
SOURCE Z:
LOAD Z:

PIN NO.   K to   J4E/E23
FUNCTION: 3 Bit Word 4 Q
VOLTAGE: 0V to 0.4V/
            2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: Test Set
SOURCE Z:
LOAD Z: ≥10 K ohms

PIN NO.   P to   J3c
FUNCTION: Common
VOLTAGE:

ORIGIN:
DESTINATION: Test Set
SOURCE Z:
LOAD Z:

PIN NO.   L to   J3b/E63
FUNCTION: ADC/DAC Analog Out
VOLTAGE: 0V to 5V DC

ORIGIN: ADC/DAC
DESTINATION: Test Set
SOURCE Z: 1 K ohms
LOAD Z: ≥ 100 K ohms

PIN NO.   R to   J5R/E100
FUNCTION: Clock Inhibit
VOLTAGE: 0V to 0.4V/
            2.4V to 5.5V DC
ORIGIN: External Source
DESTINATION: Test Set
SOURCE Z: 2 K ohms
LOAD Z: ≤ 180 Ohms

PIN NO.   M to   J1P
FUNCTION: Common
VOLTAGE:

ORIGIN:
DESTINATION: Test Set
SOURCE Z:
LOAD Z:

PIN NO.   S
FUNCTION: Chassis
VOLTAGE:

ORIGIN:
DESTINATION: Test Set
SOURCE Z:
LOAD Z:

CONNECTOR FUNCTION
TEST SET INTERFACE

PIN NO.   T to   E58
FUNCTION: Error Signal High
VOLTAGE:

ORIGIN: Filter Board
DESTINATION: Test Set
SOURCE Z:
LOAD Z:

PIN NO.   X
FUNCTION: Spare
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   U to   E59
FUNCTION: Shield
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   Y
FUNCTION: Spare
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   V to   J5E/E56
FUNCTION: Op/Non Op Q
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   Z to   E61
FUNCTION: Error Signal Low
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   W
FUNCTION: Spare
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   a to   E60
FUNCTION: Shield
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

CONNECTOR FUNCTION
TEST SET INTERFACE

PIN NO. b
FUNCTION: Spare
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO. c to J4c/E46
FUNCTION: Low Simulate
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO. d to J4d/E45
FUNCTION: High Simulate
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO. e to J4e/E48
FUNCTION: Full Probe Test
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO. f
FUNCTION: Spare
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO. g
FUNCTION: Spare
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO. h
FUNCTION: Spare
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO. j
FUNCTION: Spare
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:
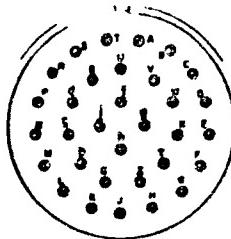
CONNECTOR FUNCTION 18-32
TEST SET INTERFACE

TITLE: 2873-545-104

MODEL: DCMS

REVISION: A

CONNECTOR: J2 AFD54-18-32SW

PIN NO.	A to E70
FUNCTION:	Counter IQ
VOLTAGE:	0 V to 0.4 V/
	2.4 V to 5.5 V DC
ORIGIN:	Up/Down Counter
DESTINATION:	Test Set E14
SOURCE Z:	
LOAD Z:	≧10 K ohms

PIN NO.	E to E74
FUNCTION:	Counter 16Q
VOLTAGE:	0 V to 0.4 V/
	2.4 V to 5.5 V DC
ORIGIN:	Up/Down Counter
DESTINATION:	Test Set E12
SOURCE Z:	
LOAD Z:	≥10 K ohms

PIN NO.	B to E71
FUNCTION:	Counter 2 Q
VOLTAGE:	0 V to 0.4 V/
	2.4V to 5.5V DC
ORIGIN:	Up/Down Counter
DESTINATION:	Test Set E15
SOURCE Z:	
LOAD Z:	≥ 10 K ohms

PIN NO.	F to E75
FUNCTION:	Counter 32 Q
VOLTAGE:	0 V to 0.4 V/
	2.4 V to 5.5V DC
ORIGIN:	Up/Down Counter
DESTINATION:	Test Set E2
SOURCE Z:	
LOAD Z:	≥ 10 K ohms

PIN NO.	C to E72
FUNCTION:	Counter 4 Q
VOLTAGE:	0 V to 0.4 V/
	2.4 V to 5.5 V DC
ORIGIN:	Up-Down Counter
DESTINATION:	Test Set E10
SOURCE Z:	
LOAD Z:	≥10 K ohms

PIN NO.	G to E64
FUNCTION:	Counter 64 Q
VOLTAGE:	0 V to 0.4 V/
	2.4 V to 5.5 V DC
ORIGIN:	Up/Down Counter
DESTINATION:	Test Set E1
SOURCE Z:	
LOAD Z:	≥10 K ohms

PIN NO.	D to E73
FUNCTION:	Counter 8 Q
VOLTAGE:	0 V to 0.4 V/
	2.4V to 5.5V DC
ORIGIN:	Up/Down Counter
DESTINATION:	Test Set E11
SOURCE Z:	
LOAD Z:	≥ 10 K ohms

PIN NO.	H to E65
FUNCTION:	Counter 128 Q
VOLTAGE:	0 V to 0.4 V/
	2.4 V to 5.5V DC
ORIGIN:	Up/Down Counter
DESTINATION:	Test Set E16
SOURCE Z:	
LOAD Z:	≥ 10 K ohms

CONNECTOR FUNCTION
TEST SET INTERFACE

PIN NO.   J   to   E66
FUNCTION: Counter 256 Q
VOLTAGE: 0V to 0.4V/
           2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: Test Set E17
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   K   to   E67
FUNCTION: Counter 512 Q
VOLTAGE: 0 to 0.4V/
           2.4V to 5.5V DC
ORIGIN   Up/Down Counter
DESTINATION: Test Set E19
SOURCE Z:
LOAD :   ≥ 10 K ohms

PIN NO.   L   to   E68
FUNCTION: Counter 1024 Q
VOLTAGE: 0 to 0.4V/
           2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: Test Set E20
SOURCE Z:
LOAD :   ≥ 10 K ohms

PIN NO.   M   to   E69
FUNCTION: Counter 2048 Q
VOLTAGE: 0V to 0.4V/
           2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: Test Set E21
SOURCE Z:
LOAD :   ≥ 10 K ohms

PIN NO.   N   to   E94
FUNCTION: Load-Counter Program
VOLTAGE: 0V to 0.4V/
           2.4V to 5.5V DC
ORIGIN: Counter
DESTINATION: Test Set
SOURCE Z: 900 ohms
LOAD Z: ≤ 75 ohms

PIN NO.   P   to   E76
FUNCTION: Counter Program 1
VOLTAGE: 0V to 0.4V/
           2.4V to 5.5V DC
ORIGIN: Counter
DESTINATION: Test Set
SOURCE Z: 2 K ohms
LOAD Z: ≤ 180 ohms

PIN NO.   R   to   E79
FUNCTION: Counter Program 2
VOLTAGE: 0V to 0.4V/
           2.4V to 5.5V DC
ORIGIN: Counter
DESTINATION: Test Set
SOURCE Z: 2 K ohms
LOAD Z: ≤ 180 ohms

PIN NO.   S   to   E77
FUNCTION: Counter Program 4
VOLTAGE: 0V to 0.4V/
           2.4V to 5.5V DC
ORIGIN: Counter
DESTINATION: Test Set
SOURCE Z: 2 K ohms
LOAD Z: ≤ 180 ohms

CONNECTOR FUNCTION
TEST SET INTERFACE

PIN NO.   T   to   E78
FUNCTION: Counter Program 8
VOLTAGE: 0V to 0.4V/
                    2.4V to 5.5V DC
ORIGIN: Counter
DESTINATION: Test Set
SOURCE Z: 2 K ohms
LOAD Z: ≤ 180 Ohms

PIN NO.   X   to   E97
FUNCTION: Counter Program 64
VOLTAGE: 0V to 0.4V/
                    2.4V to 5.5V DC
ORIGIN: Counter
DESTINATION: Test Set
SOURCE Z: 2 K ohms
LOAD Z: ≤ 180 ohms

PIN NO.   U   to   E98
FUNCTION: Counter Program 16
VOLTAGE: 0V to 0.4V/
                    2.4V to 5.5V DC
ORIGIN: Counter
DESTINATION: Test Set
SOURCE Z: 2 K ohms
LOAD Z: ≤ 180 ohms

PIN NO.   Y   to   E121
FUNCTION: Counter Program 256
VOLTAGE: 0V to 0.4V/
                    2.4V to 5.5V DC
ORIGIN: Counter
DESTINATION: Test Set
SOURCE Z: 2 K ohms
LOAD Z: ≤180 ohms

PIN NO.   V   to   E95
FUNCTION: Counter Program 32
VOLTAGE: 0V to 0.4V/
                    2.4V to 5.5V DC
ORIGIN: Counter
DESTINATION: Test Set
SOURCE Z: 2 K ohms
LOAD Z: ≤180 ohms

PIN NO.   Z   to   E122
FUNCTION: Counter Program 512
VOLTAGE: 0V to 0.4V/
                    2.4V to 5.5V DC
ORIGIN: Counter
DESTINATION: Test Set
SOURCE Z: 2 K ohms
LOAD Z: ≤180 ohms

PIN NO.   W   to   E96
FUNCTION: Counter Program 128
VOLTAGE: 0V to 0.4V/
                    2.4V to 5.5V DC
ORIGIN: Counter
DESTINATION: Test Set
SOURCE Z: 2 K ohms
LOAD Z: ≤180 ohms

PIN NO.   a   to   E120
FUNCTION: Counter Program 1024
VOLTAGE: 0V to 0.4V/
                    2.4V to 5.5V DC
ORIGIN: Counter
DESTINATION: Test Set
SOURCE Z: 2 K ohms
LOAD Z: ≤180 ohms

CONNECTOR FUNCTION
TEST SET INTERFACE

PIN NO.   b   to   E119
FUNCTION: Counter Program 2048
VOLTAGE: 0V to 0.4V/
           2.4V to 5.5V DC
ORIGIN: Counter
DESTINATION: Test Set
SOURCE Z: 2 K ohms
LOAD Z: ≤180 ohms

PIN NO.   f   to   J4f/E47
FUNCTION: ∅ Det Out
VOLTAGE:
ORIGIN: ∅ Det
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   c   to   J2d
FUNCTION: Common
VOLTAGE:

ORIGIN:
DESTINATION: Test Set
SOURCE Z:
LOAD Z:

PIN NO.   g
FUNCTION: Spare
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   d   to   E124
FUNCTION: Common
VOLTAGE:

ORIGIN:
DESTINATION: Test Set
SOURCE Z:
LOAD Z:

PIN NO.   h
FUNCTION: Spare
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   e
FUNCTION:. Chassis
VOLTAGE:

ORIGIN:
DESTINATION: Test Set
SOURCE Z:
LOAD Z:

PIN NO.   j
FUNCTION: Spare
VOLTAGE: -

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:
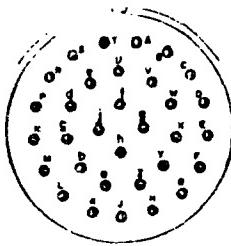
CONNECTOR FUNCTION 18-32
COUNTER/OUTPUT

TITLE: 2873-545-104

MODEL: DCMS

REVISION: A

CONNECTOR: J3 AFD54-18-32PN

PIN NO. A to E81
FUNCTION: Counter 1 Q
VOLTAGE: 0V to 0.4V/
2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥10 K ohms

PIN NO. E to E85
FUNCTION: Counter 4 Q
VOLTAGE: 0V to 0.4V/
2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥10 K ohms

PIN NO. B to $\overline{E80}$
FUNCTION: Counter 1 $\overline{Q}$
VOLTAGE: 0V to 0.4V/
2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥10 K ohms

PIN NO. F to $\overline{E84}$
FUNCTION: Counter 4 $\overline{Q}$
VOLTAGE: 0V to 0.4V/
2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥10 K ohms

PIN NO. C to E83
FUNCTION: Counter 2 Q
VOLTAGE: 0V to 0.4V/
2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥10 K ohms

PIN NO. G to E87
FUNCTION: Counter 8 Q
VOLTAGE: 0V to 0.4V/
2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥10 K ohms

PIN NO. D to $\overline{E82}$
FUNCTION: Counter 2 $\overline{Q}$
VOLTAGE: 0V to 0.4V/
2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥10 K ohms

PIN NO. H to $\overline{E86}$
FUNCTION: Counter 8 $\overline{Q}$
VOLTAGE: 0V to 0.4V
2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥10 K ohms

CONNECTOR FUNCTION
TEST SET INTERFACE

PIN NO.   J   to   E89
FUNCTION: Counter 16 Q
VOLTAGE: 0V to 0.4V/
           2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   K   to   E88
FUNCTION: Counter 16 Q
VOLTAGE: 0V to 0.4V/
           2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   L   to   E91
FUNCTION: Counter 32 Q
VOLTAGE: 0V to 0.4V/
           2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   M   to   E90
FUNCTION: Counter 32 Q
VOLTAGE: 0V to 0.4V/
           2.4V to 5.5V DC
ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   N   to   E104
FUNCTION: Counter 64 Q
VOLTAGE: 0V to 0.4V/
           2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   P   to   E103
FUNCTION: Counter 64 Q
VOLTAGE: 0V to 0.4V/
           2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   R   to   E106
FUNCTION: Counter 128 Q
VOLTAGE: 0V to 0.4V/
           2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   S   to   E105
FUNCTION: Counter 128 Q
VOLTAGE: 0V to 0.4V/
           2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

CONNECTOR FUNCTION
COUNTER/OUTPUT

PIN NO.   T   to   E108
FUNCTION: Counter 256 Q
VOLTAGE: 0V to 0.4V/
                    2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   U   to   E107
FUNCTION: Counter 256 $\overline{Q}$
VOLTAGE: 0V to 0.4V/
                    2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   V   to   E110
FUNCTION: Counter 512 Q
VOLTAGE: 0V to 0.4V/
                    2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   W   to   E109
FUNCTION: Counter 512 $\overline{Q}$
VOLTAGE: 0V to 0.4V/
                    2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: . ≥ 10 K ohms

PIN NO.   X   to   E112
FUNCTION: Counter 1024 Q
VOLTAGE: 0V to 0.4V/
                    2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   Y   to   E111
FUNCTION: Counter 1024 $\overline{Q}$
VOLTAGE: 0V to 0.4V
                    2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   Z   to   E114
FUNCTION: Counter 2048 Q
VOLTAGE: 0V to 0.4V/
                    2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   a   to   E113
FUNCTION: Counter 2048 $\overline{Q}$
VOLTAGE: 0V to 0.4V/
                    2.4V to 5.5V DC
ORIGIN: Up/Down Counter
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

TITLE: 2873-545-104

MODEL: DCMS

CONNECTOR FUNCTION
COUNTER/OUTPUT

REVISION: A

CONNECTOR: J3 AFD54-18-32 PN

PIN NO.   b   to   E63
FUNCTION: ADC/DAC Analog Out
VOLTAGE: 0V to 5V DC

ORIGIN: ADC/DAC
DESTINATION: System Interface
SOURCE Z: 1 K ohms
LOAD Z: ≥ 100 K ohms

PIN NO.   c   to   j3e
FUNCTION: Common
VOLTAGE:

ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.   d   to   E62
FUNCTION: ADC/DAC Ref. Out
VOLTAGE: 5 V DC

ORIGIN: ADC/DAC
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.   e   to   J5N
FUNCTION: Common
VOLTAGE:

ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.   f
FUNCTION: Chassis
VOLTAGE:

ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.   g
FUNCTION: Spare
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   h
FUNCTION: Spare
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   j
FUNCTION: Spare
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

TITLE: 2873-545-104

MODEL: DCMS

CONNECTOR FUNCTION 15-32

POINT SENSOR OUTPUT

REVISION: A

CONNECTOR: J4 AFD54-18-32PW

PIN NO.	A to E19	
FUNCTION:	3 Bit Word 1 Q	
VOLTAGE:	0V to 0.4V/	
	2.4 V to 5.5V DC	
ORIGIN:	Point Sensor	
DESTINATION:	System Interface	
SOURCE Z:		
LOAD Z:	≥ 10 K ohms	

PIN NO.   E to   E23
FUNCTION·   3 Bit Word 4 Q
VOLTAGE: 0V to 0.4V/
             2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   B to   E17
FUNCTION: 3 Bit Word 1 $\overline{Q}$
VOLTAGE: 0 V to 0.4 V/
             2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥10 K ohms

PIN NO.   F to   E20
FUNCTION: 3 Bit Word 4 $\overline{Q}$
VOLTAGE: 0 V to 0.4 V/
             2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥10 K ohms

PIN NO.   C to   E21
FUNCTION: 3 Bit Word 2 Q
VOLTAGE: 0 V to 0.4 V/
             2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   G to   E16
FUNCTION·   Point Sensor 1 Q
VOLTAGE: 0 V to 0.4 V/
             2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   D to   E18
FUNCTION: 3 Bit Word 2 $\overline{Q}$
VOLTAGE: 0V to 0.4V/
             2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥10 K ohms

PIN NO.   H to   E14
FUNCTION: Point Sensor 1 $\overline{Q}$
VOLTAGE: 0V to 0.4V/
             2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥10 K ohms

CONNECTOR FUNCTION
POINT SENSOR OUTPUT

PIN NO.   J   to   E15
FUNCTION: Point Sensor 2 Q
VOLTAGE: 0V to 0.4V/
                2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   B   to   E8
FUNCTION: Point Sensor 4 Q
VOLTAGE: 0V to 0.4V/
                2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   K   to   E13
FUNCTION: Point Sensor 2 $\overline{Q}$
VOLTAGE: 0V to 0.4V/
                2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   P   to   E9
FUNCTION: Point Sensor 4 $\overline{Q}$
VOLTAGE: 0V to 0.4V/
                2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   L   to   E11
FUNCTION: Point Sensor 3 Q
VOLTAGE: 0V to 0.4V/
                2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   R   to   E7
FUNCTION: Point Sensor 5 Q
VOLTAGE: 0V to 0.4V/
                2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   M   to   E12
FUNCTION: Point Sensor 3 $\overline{Q}$
VOLTAGE: 0V to 0.4V/
                2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

PIN NO.   S   to   E10
FUNCTION: Point Sensor 5 $\overline{Q}$
VOLTAGE: 0V to 0.4V/
                2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥ 10 K ohms

CONNECTOR FUNCTION
POINT SENSOR OUTPUT

PIN NO.   T   to   E24
FUNCTION: Point Sensor 6 Q
VOLTAGE: 0V to 0.4V/
            2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥10 K ohms

PIN NO.   X   to   FL2
FUNCTION: -28 V in
VOLTAGE:
ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.   U   to   E22
FUNCTION: Point Sensor 6 $\overline{Q}$
VOLTAGE: 0V to 0.4V/
            2.4V to 5.5V DC
ORIGIN: Point Sensor
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ≥10 K ohms

PIN NO.   Y   to   FL2
FUNCTION: -28 V in
VOLTAGE:
ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.   V   to   FL1
FUNCTION: +28 V in
VOLTAGE:
ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.   Z   to   J4a
FUNCTION: Common
VOLTAGE:
ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.   W   to   FL1
FUNCTION: +28 V in
VOLTAGE:
ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.   a   to   J2c/J4Z
FUNCTION: Common
VOLTAGE:
ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

CONNECTOR FUNCTION
POINT SENSOR OUTPUT

PIN NO.   b
FUNCTION: Chassis
VOLTAGE:

ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.   c   to   J1c
FUNCTION: Low Simulate
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   d   to   J1d
FUNCTION: High Simulate
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   e   to   J1e
FUNCTION: Full Probe Test
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   f   to   E47
FUNCTION: $\emptyset$ Det Output
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   g
FUNCTION: Spare
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   h
FUNCTION: Spare
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   j
FUNCTION: Spare
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:
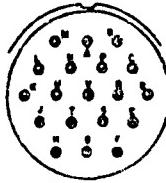
TITLE: 2873-545-104

MODEL: DCMS

CONNECTOR FUNCTION   14-19   REVISION: A

HEALTH MONITOR

CONNECTOR: J5 AFD54-14-19PN

PIN NO.	A to E117
FUNCTION:	Below Range Inh. Q
VOLTAGE:	0V to 0.4V/
	2.4V to 5.5V DC
ORIGIN:	Up/Down Counter
DESTINATION:	System Interface
SOURCE Z:	
LOAD Z:	≥ 10 K ohms

PIN NO.	E to E56
FUNCTION:	Op/Non-Op Q
VOLTAGE:	0V to 0.4V/
	2.4V to 5.5V DC
ORIGIN:	Health Monitor
DESTINATION:	System Interface
SOURCE Z:	
LOAD Z:	≥10 K ohms

PIN NO.	B to E118
FUNCTION:	Below Range Inh. $\overline{Q}$
VOLTAGE:	0V to 0.4V/
	2.4V to 5.5V DC
ORIGIN:	Up/Down Counter
DESTINATION:	System Interface
SOURCE Z:	
LOAD Z:	≥ 10K ohms

PIN NO.	F to E55
FUNCTION:	Op/Non-Op $\overline{Q}$
VOLTAGE:	0V to 0.4V/
	2.4 V to 5.5V DC
ORIGIN:	Health Monitor
DESTINATION:	System Interface
SOURCE Z:	
LOAD Z:	≥10K ohms

PIN NO.	C to E115
FUNCTION:	Overrange Inh. Q
VOLTAGE:	0V to 0.4 V/
	2.4 V to 5.5V DC
ORIGIN:	Up/Down Counter
DESTINATION:	System Interface
SOURCE Z:	
LOAD Z:	≥ 10 K ohms

PIN NO.	G to E51
FUNCTION:	Health Mon-Pwr Sup Q
VOLTAGE:	0V to 0.4V/
	2.4V to 5.5V DC
ORIGIN:	Health Monitor
DESTINATION:	System Interface
SOURCE Z:	
LOAD Z:	≥ 10 K ohms

PIN NO.	D to E116
FUNCTION:	Over Range Inh. $\overline{Q}$
VOLTAGE:	0 V to 0.4 V/
	2.4 V to 5.5 V DC
ORIGIN:	Up/Down Counter
DESTINATION:	System Interface
SOURCE Z:	
LOAD Z:	≥ 10 K ohms

PIN NO.	H to E52
FUNCTION:	Health Mon-Pwr Sup $\overline{Q}$
VOLTAGE:	0 V to 0.4 V/
	2.4 V to 5.5 V DC
ORIGIN:	Health Monitor
DESTINATION:	System Interface
SOURCE Z:	
LOAD Z:	≥ 10 K ohms

CONNECTOR FUNCTION
HEALTH MONITOR

PIN NO. J to E49	PIN NO. N to J5P
FUNCTION: Health Mon-Bridge Osc	FUNCTION: Common
VOLTAGE: Q 0V to 0.4V/	VOLTAGE:
2.4V to 5.5 V DC	
ORIGIN: Health Monitor	ORIGIN:
DESTINATION: System Interface	DESTINATION: System Interface
SOURCE Z:	SOURCE Z:
LOAD Z: $\geq$ 10 K ohms	LOAD Z:

PIN NO. K to E54	PIN NO. P to J4Z
FUNCTION: Health Mon-Bridge	FUNCTION: Common
Osc Q	
VOLTAGE: 0V to 0.4V/	VOLTAGE:
2.4V to 5.5V DC	
ORIGIN: Health Monitor	ORIGIN:
DESTINATION: System Interface	DESTINATION: System Interface
SOURCE Z:	SOURCE Z:
LOAD Z: $\geq$ 10 K ohms	LOAD Z:

PIN NO. L to E50	PIN NO. R to J1R
FUNCTION: Health Mon-Clock Q	FUNCTION: Clock Inhibit
VOLTAGE: 0V to 0.4V/	VOLTAGE: 0V to 0.4V/
2.4V to 5.5V DC	2.4V to 5.5V DC
ORIGIN: Health Monitor	ORIGIN: External Source
DESTINATION: System Interface	DESTINATION: System Interface
SOURCE Z:	SOURCE Z:
LOAD Z: $\geq$ 10 K ohms	LOAD Z:

PIN NO. M to E53	PIN NO. S
FUNCTION: Health-Mon-Clock $\overline{Q}$	FUNCTION: Chassis
VOLTAGE: 0V to 0.4V/	VOLTAGE:
2.4V to 5.5V DC	
ORIGIN: Health Monitor	ORIGIN:
DESTINATION: System Interface	DESTINATION: System Interface
SOURCE Z:	SOURCE Z:
LOAD Z: $\geq$ 10 K ohms	LOAD Z:

CONNECTOR FUNCTION
HEALTH MONITOR

PIN NO.   T
FUNCTION: Spare
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   U
FUNCTION: Spare
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

TITLE: 2873-545-104

MODEL: DCMS

CONNECTOR FUNCTION
UNKNOWN INPUT

REVISION: A

CONNECTOR: J6   TNC   KA 7959

PIN NO.   Center Conductor to E44 PIN NO.
FUNCTION: Unknown Input   FUNCTION:
VOLTAGE: VOLTAGE:

ORIGIN: ORIGIN:
DESTINATION: System Interface   DESTINATION:
SOURCE Z: SOURCE Z:
LOAD Z: ·   LOAD Z:

PIN NO.   Shield   to E42   PIN NO.
FUNCTION: Common   FUNCTION:
VOLTAGE: VOLTAGE:

ORIGIN: ORIGIN:
DESTINATION: System Interface   DESTINATION:
SOURCE Z: SOURCE Z:
LOAD Z: LOAD Z:

PIN NO.   PIN NO.
FUNCTION: FUNCTION:
VOLTAGE: VOLTAGE:

ORIGIN: ORIGIN:
DESTINATION: DESTINATION:
SOURCE Z: SOURCE Z:
LOAD Z: LOAD Z:

PIN NO.   PIN NO.
FUNCTION: FUNCTION:
VOLTAGE: VOLTAGE:

ORIGIN: ORIGIN:
DESTINATION: DESTINATION:
SOURCE Z: SOURCE Z:
LOAD Z: LOAD Z:

TITLE: 2873-545-104

MODEL: DCMS

CONNECTOR FUNCTION   REVISION: A
REFERENCE INPUT
                            CONNECTOR: J7 TNC KA7959

PIN NO.   Center Conductor to E43   PIN NO.
FUNCTION: Reference Input   FUNCTION:
VOLTAGE: VOLTAGE:

ORIGIN: ORIGIN:
DESTINATION: System Interface   DESTINATION:
SOURCE Z: SOURCE Z:
LOAD Z: ·   LOAD Z:

PIN NO.   Shield   to E41   PIN NO.
FUNCTION: Common   FUNCTION:
VOLTAGE: VOLTAGE:

ORIGIN: ORIGIN:
DESTINATION: System Interface   DESTINATION:
SOURCE Z: SOURCE Z:
LOAD Z: LOAD Z:

PIN NO.   PIN NO
FUNCTION: FUNCTION:
VOLTAGE: VOLTAGE:

ORIGIN: ORIGIN:
DESTINATION: DESTINATION:
SOURCE Z: SOURCE Z:
LOAD Z: LOAD Z:

PIN NO.   PIN NO.
FUNCTION: FUNCTION:
VOLTAGE: VOLTAGE:

ORIGIN: ORIGIN:
DESTINATION: DESTINATION:
SOURCE Z: SOURCE Z:
LOAD Z: LOAD Z:

CONNECTOR FUNCTION
BRIDGE OSC OUTPUT

PIN NO. Center Conductor to E35
FUNCTION: Bridge Osc E +
VOLTAGE:

ORIGIN: Bridge Oscillator
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.   Shield   to E32
FUNCTION: Common
VOLTAGE:

ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z.

CONNECTOR FUNCTION
BRIDGE OSC OUTPUT

PIN NO. Center Conductor to E34
FUNCTION: Bridge Osc E-
VOLTAGE:

ORIGIN: Bridge Oscillator
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.   Shield   to E31
FUNCTION: Common
VOLTAGE:

ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

CONNECTOR FUNCTION
POINT SENSOR INPUT

PIN NO. Center Conductor to E25
FUNCTION: Point Sensor #1
VOLTAGE:

ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO. Shield to E26
FUNCTION: Commor
VOLTAGE:

ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

CONNECTOR FUNCTION
POINT SENSOR INPUT

PIN NO. Center Conductor to E27
FUNCTION: Point Sensor #2
VOLTAGE:

ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.   Shield   to   E28
FUNCTION: Common
VOLTAGE:

ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

CONNECTOR FUNCTION
POINT SENSOR INPUT

PIN NO. Center Conductor to E29   PIN NO.
FUNCTION: Point Sensor #3   FUNCTION:
VOLTAGE: VOLTAGE:

ORIGIN: ORIGIN:
DESTINATION: System Interface   DESTINATION:
SOURCE Z: SOURCE Z:
LOAD Z: LOAD Z:

PIN NO.   Shield   to   E30   PIN NO.
FUNCTION: Common   FUNCTION:
VOLTAGE: VOLTAGE:

ORIGIN: ORIGIN:
DESTINATION: System Interface   DESTINATION:
SOURCE Z: SOURCE Z:
LOAD Z: LOAD Z:

PIN NO.   PIN NO.
FUNCTION: FUNCTION:
VOLTAGE: VOLTAGE:

ORIGIN: ORIGIN:
DESTINATION: DESTINATION:
SOURCE Z: SOURCE Z:
LOAD Z: LOAD Z:

PIN NO.   PIN NO.
FUNCTION: FUNCTION:
VOLTAGE: VOLTAGE:

ORIGIN: ORIGIN:
DESTINATION: DESTINATION:
SOURCE Z: SOURCE Z:
LOAD Z: LOAD Z:

TITLE: 2873-545-104

MODEL: DCMS

CONNECTOR FUNCTION
POINT SENSOR INPUT

REVISION: A

CONNECTOR: J13   TNC   KA7959

PIN NO.   Center Conductor to E5
FUNCTION: Point Sensor #4
VOLTAGE:

ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.   Shield   to   E6
FUNCTION: Common
VOLTAGE:

ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

G

CONNECTOR FUNCTION
POINT SENSOR INPUT

PIN NO.   Center Conductor to E1
FUNCTION: Point Sensor #5
VOLTAGE:

ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.   Shield   to E2
FUNCTION: Common
VOLTAGE:

ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

CONNECTOR FUNCTION
POINT SENSOR INPUT

PIN NO.   Center Conductor to E3
FUNCTION: Point Sensor #6
VOLTAGE:

ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z: ·

PIN NO.   Shield   to   E4
FUNCTION: Common
VOLTAGE:

ORIGIN:
DESTINATION: System Interface
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

PIN NO.
FUNCTION:
VOLTAGE:

ORIGIN:
DESTINATION:
SOURCE Z:
LOAD Z:

4.2.2 MECHANICAL

4.2.2.1 Construction

The DCMS unit is modular in design permitting easy removal of PC Board Assemblies. The PC Board Assemblies are conformal coated for environmental protection.

4.2.2.2 Size

The DCMS unit has a volume of 360 cubic inches not including mounting bosses or connector protrusions. The unit is 6 inches wide by 6.5 inches high by 9.2 inches long.

4.2.2.3 Weight

The weight of the DCMS unit is 12 pounds maximum.

4.2.2.4 Connector

The DCMS unit has 15 connectorsmounted on the top surface. The 15 connectors consist of 10 co-axial connectors and 5 multi-pin connectors.

5.0   ENGINEERING MODELS

The hardware phase of the contract consisted of a breadboard and three engineering models. The breadboard was used to prove out the basic design as well as the multi-mode aspects of the DCMS unit. Three engineering units were then fabricated incorporating specific modes of operation. These modes are delineated below.

ENGINEERING MODEL NO. 1

Operation Mode - Absolute Capacitance

Operating Range

        Continuous - 60 to 70 pf

        Discrete   - 5 to 8 pf (5.5 pf threshold switch point)

Bridge Excitation Frequency - 90 kHz

Continuous digital output - 12 bits

Continuous Bridge input impedance - 5 ohms

Counter clock free-running frequency - 100 Hz

Maximum Sync frequency - 2.5 kHz

ENGINEERING MODEL NO. 2

Operation Mode - Absolute Capacitance

Operating Range

        Continuous - 100 to 120 pf

        Discrete   - 5 to 8 pf (5.5 pf threshold switch point)

Bridge Excitation Frequency - 60 kHz

Continuous digital output - 12 bits

Continuous Bridge input impedance - 5 ohms

Counter clock free-running frequency - 100 Hz

Maximum Sync Frequency - 2.5 kHz

ENGINEERING MODEL NO. 3

Operation Mode - Capacitance Difference

Operating Range

        Continuous $\pm$ 20 pf probes capacitance 400-800 pf

        Discrete - 5 to 8 pf (5.5 pf threshold switch point)

Bridge Excitation Frequency - 30 kHz

Continuous digital output - 12 bits

Continuous Bridge input impedance - 5 ohms

Counter clock free-running frequency - 100 Hz

Maximum Sync Frequency - 2.5 kHz

All three engineering units were thermally tested and performance monitored using the DCMS Test Set. The result of these tests are included in this section. Based on these tests, the electrical design goals were reached and successfully demonstrated.
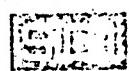
Range __ 60 - 70 pf __   Freq. __ 90 KHZ __

Analog Output (volts) for Indicated Count

Count	-40°C	-20°C	25°C	71°C	Remarks
0	.0140	.0088	.0010	.0052	
200	.2581	.2530	.2433	.2390	
400	.5020	.4968	.4870	.4825	
600	.7463	.7408	.7310	.7264	
800	.9902	.9850	.9748	.9704	
1000	1.2344	1.2293	1.2188	1.2146	
1200	1.4785	1.4736	1.4633	1.4590	
1400	1.7224	1.7144	1.7070	1.7025	
1600	1.9670	1.9622	1.9518	1.9477	
1800	2.2105	2.2058	2.1952	2.1910	
2000	2.4546	2.4500	2.4395	2.4354	
2200	2.6977	2.6930	2.6825	2.6785	
2400	2.9418	2.9373	2.9266	2.9227	
2600	3.1857	3.1810	3.1702	3.1664	
2800	3.4297	3.4253	3.4145	3.4107	
3000	3.673	3.6688	3.6578	3.6542	
3200	3.9178	3.9138	3.9030	3.8998	
3400	4.1615	4.1573	4.1465	4.1435	
3600	4.4053	4.4012	4.3905	4.3873	
3800	4.6493	.6452	4.6344	4.6314	
4000	4.8933	4.8893	4.8783	4.8753	
4095	5.0080	5.0041	4.9928	4.9900	
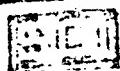
SCI SYSTEMS, INC.

TITLE _____ DCMS _____

MODEL _____ 2873000-1 _____

REVISION DATE _____ PAGE 2 OF 3

Serial No. _001_

Range 60 -70 pf   Freq. 90 kHz   Cable Length 5 FT

Probe Capacitance (pf) for Indicated Count

Count	-40°C	-20°C	25°C	71°C	Remarks
0	60.076	60.032	60.000	60.056	
200	60.570	60.528	60.501	60.554	
400	61.062	61.026	61.001	61.047	
600	61.558	61.524	61.501	61.543	
800	62.048	62.021	62.000	62.036	
1000	62.541	62.518	62.500	62.529	
1200	63.034	63.016	63.006	63.022	
1400	63.523	63.512	63.500	63.518	
1600	64.021	64.010	64.000	64.012	
1800	64.513	64.507	64.500	64.505	
2000	65.007	65.004	64.999	64.999	
2200	65.499	65.502	65.498	65.492	
2400	65.992	66.000	65.999	65.986	
2600	66.484	66.497	66.498	66.478	
2800	66.978	66.994	66.999	66.973	
3000	67.469	67.492	67.499	67.465	
3200	67.962	67.988	67.998	67.958	
3400	68.454	68.486	68.497	68.451	
3600	68.947	68.982	68.997	68.944	
3800	69.431	69.479	69.495	69.436	
4000	69.937	69.977	69.996	69.928	
4095	—	—	—	—	—
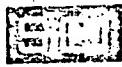
SCI FORM 810-032   DATE FEB 21, 1973   TAKEN BY: L CAMPBELL

Freq. 90 kHz   Cable Length 5 ft.

Point Sensor Threshold Capacitance

Sensor	-40°C	-20°C	25°C	71°C	Remarks
1	5.551	5.548	5.536	5.532	
2	5.535	5.536	5.529	5.536	
3	5.534	5.536	5.526	5.542	
4	5.560	5.558	5.534	5.542	
5	5.542	5.532	5.511	5.542	
6	5.550	5.551	5.515	5.543	

Level Simulation Test

Test	Read Out Count				
Low	202	200	200	201	
High	3648	3618	3603	3646	
Full	3895	3898	3898	3896	

DATE: FEB 21 1973   TAKEN BY: L. CAMPBELL

SCI SYSTEMS, INC.

Range _100pf to 120pf_____   Freq. _60KHz_____

Analog Output (volts) for Indicated Count

Count	-40°C	-20°C	25°C	71°C	Remarks
0	+.0056	+.0047	+.0018	-.0022	
200	.2516	.2503	.2468	+.2417	
400	.4966	.4949	.4903	.4840	
600	.7417	.7396	.7340	.7267	
800	.9868	.9841	.9777	.9690	
1000	1.2328	1.2300	1.2225	1.2129	
1200	1.4768	1.4723	1.4698	1.4537	
1400	1.7223	1.7185	1.7091	1.6968	
1600	1.9671	1.9630	1.9526	1.9392	
1800	2.2123	2.2078	2.1963	2.1817	
2000	2.4583	2.4536	2.4413	2.4257	
2200	2.17010	2.6957	2.6818	2.6647	
2400	2.9465	2.9407	2.9260	2.9078	
2600	3.1913	3.1850	3.1690	3.1494	
2800	3.4373	3.4307	3.4140	3.3935	
3000	3.6823	3.6750	3.6575	3.6360	
3200	3.9265	3.9192	3.9002	3.8770	
3400	4.1720	4.1645	4.1443	4.1200	
3600	4.4167	4.4090	4.3873	4.3620	
3800	4.6630	4.6548	4.6322	4.6058	
4000	4.9080	4.8994	4.8760	4.8480	
4095	5.0250	5.0165	4.9924	4.9640	

SCI SYSTEMS, INC.

TITLE	DCMS
MODEL	2873000-1
REVISION DATE	PAGE 2 OF 3
Serial No.	002

Range _100pf to 120pf_ Freq. _60KHz_ Cable Length _5ft._

Probe Capacitance (pf) for Indicated Count

Count	-40°C	-20°C	25°C	71°C	Remarks
0	99.850	99.860	100.000	100.300	
200	100.845	100.855	101.000	101.280	
400	101.840	101.855	102.000	102.260	
600	102.835	102.855	103.005	103.235	
800	103.830	103.850	104.005	104.215	
1000	104.825	104.855	105.005	105.195	
1200	105.820	105.850	106.005	106.175	
1400	106.810	106.845	107.010	107.150	
1600	107.800	107.845	108.010	108.125	
1800	108.795	108.845	109.010	109.100	
2000	109.790	109.840	110.015	110.075	
2200	110.795	110.850	111.020	111.060	
2400	111.780	111.845	112.020	112.035	
2600	112.780	112.845	113.025	113.015	
2800	113.770	113.845	114.025	113.985	
3000	114.765	114.840	115.025	114.965	
3200	115.760	115.840	116.030	115.940	
3400	116.755	116.840	117.030	116.920	
3600	117.750	117.845	118.035	117.900	
3800	118.740	118.835	119.035	118.865	
4000	119.740	119.840	120.035	119.850	
4095	—	—	—	—	—

SCI FORM 810-032   DATE _April 5, 1973_   TAKEN BY: _L. CAMPBELL_
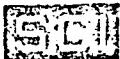
SCI SYSTEMS, INC.

TITLE _____ DCMS _____

MODEL _____ 2873000-1 _____

REVISION DATE _____ PAGE 3 OF 3

Serial No. _002_

Freq. _60 KHz_   Cable Length _5 ft_

Point Sensor Threshold Capacitance

Sensor	-40°C	-20°C	25°C	71°C	Remarks
1	5.487	5.494	5.494	5.480	
2	5.460	5.474	5.480	5.448	
3	5.484	5.498	5.502	5.470	
4	5.476	5.492	5.504	5.473	
5	5.492	5.504	5.512	5.482	
6	5.491	5.505	5.512	5.488	

Level Simulation Test

Test	Read Out Count				
Low	201	200	198	206	
High	3627	3610	3599	3693	
Full	3894	3896	3899	3897	

DATE: _April 5 1973_   TAKEN BY: _L. CAMPBELL_

SCI

SCI SYSTEMS, INC.

TITLE _____ DCMS

MODEL ___ 2873000-1

REVISION DATE _____ PAGE _1_ OF _3_

Serial No. 003

Range ___ ±20pf ___   Freq. ___ 30 KHz ___

Analog Output (volts) for Indicated Count

Count	-40°C	-20°C	25°C	71°C	Remarks
0	+.0027	+.0014	.0000	-.0030	
200	.2480	.2466	.2408	+.2417	
400	.4920	.4906	.4876	.4849	
600	.7363	.7348	.7315	.7283	
800	.9804	.9790	.9753	.9716	
1000	1.2255	1.2241	1.2175	1.2163	
1200	1.4684	1.4670	1.4627	1.4580	
1400	1.7130	1.7116	1.7073	1.7020	
1600	1.9570	1.9554	1.9509	1.9450	
1800	2.2010	2.1994	2.1949	2.1885	
2000	2.4431	2.4446	2.4400	2.4330	
2200	2.6890	2.6867	2.6815	2.6740	
2400	2.9337	2.9313	2.9230	2.9180	
2600	3.1772	3.1747	3.1690	3.1604	
2800	3.4223	3.4200	3.4140	3.4050	
3000	3.6664	3.6640	3.6580	3.6484	
3200	3.9074	3.9069	3.9005	3.8900	
3400	4.1536	4.1516	4.1450	4.1344	
3600	4.3970	4.3950	4.3883	4.3768	
3800	4.6422	4.6401	4.6335	4.6215	
4000	4.8875	4.8844	4.8773	4.8648	
4095	5.0018	4.9998	4.9920	4.9791	

SCI FORM 810-032   DATE _April 5, 1973_ TAKEN BY: _L. CAMPBELL_
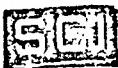
SCI SYSTEMS, INC.

TITLE _____ DCMS _____

MODEL ___ 2873000-1 ___

REVISION DATE _____ PAGE 2 OF 3

Serial No. 003

Range ±20 pf   Freq. 30KHz   Cable Length 5 ft.

Probe Capacitance (pf) for Indicated Count

Count	-40°C	-20°C	25°C	71°C	Remarks
0	-20.240	-20.240	-20.010	-19.800	
200	-18.220	-18.205	-18.015	-17.820	
400	-16.205	-16.160	-16.015	-15.845	
600	-14.170	-14.115	-14.010	-13.875	
800	-12.155	-12.075	-12.010	-11.900	
1000	-10.135	-10.015	-10.015	-9.920	
1200	-8.110	-7.985	-8.000	-7.960	
1400	-6.095	-5.945	-6.000	-5.995	
1600	-4.075	-3.915	-4.005	-4.025	
1800	-2.055	-1.875	-2.000	-2.050	
2000	-0.035	+0.165	0.000	-0.080	
2200	1.980	2.205	2.000	1.885	
2400	4.010	4.255	4.000	3.860	
2600	6.030	6.285	6.000	5.830	
2800	8.050	8.335	8.000	7.800	
3000	10.065	10.370	10.005	9.770	
3200	12.075	12.415	12.010	11.745	
3400	14.105	14.460	14.010	13.710	
3600	16.120	16.495	16.005	15.695	
3800	18.145	18.540	18.015	17.660	
4000	20.165	20.580	20.015	19.635	
4095	———	———	———	———	———

SCI FORM 810-032   DATE April 5, 197?   TAKEN BY: L. Campbell

SCI

SCI SYSTEMS, INC.

Freq. ___ 30 kHz ___   Cable Length ___ 5 ft. ___

Point Sensor Threshold Capacitance

Sensor	-40°C	-20°C	25°C	71°C	Remarks
1	5.632	5.617	5.495	5.400	
2	5.618	5.595	5.468	5.363	
3	5.635	5.615	5.514	5.427	
4	5.582	5.562	5.454	5.340	
5	5.622	5.604	5.505	5.415	
6	5.673	5.653	5.542	5.427	

Level Simulation Test

Test	Read Out Count				
Low	2185	2194	2204	2194	
High	1798	1802	1802	1802	
Full	———	———	———	———	

DATE: ___ April 5 ___   TAKEN BY: ___ L. CAMPBELL ___

SCI FORM 810-032

C^2

6.0 DCMS DISPLAY UNIT

The DCMS Display Unit is designed to provide a digital display of capacitance measurements of the DCMS unit. Twelve LED lamps are used to indicate the output state of each counter. A four digit decimal display is also provided. Three LED lamps are used to indicate the point sensor probe data. Six other LED lamps are used to indicate below range, over range, bridge oscillator, clock oscillator, power supply, and an operate/non-operate condition. The display unit also provides a provision to program the counter to any number between zero and 4095. This may be accomplished by setting the Operate/Calibrate switch (S13 on DCMS Display Schematic drawing number 2873100) to calibrate. This allows switches S1 thru S12 to set each stage of the counter to a "1" or "0" output state. Closing S12 would indicate 2048 on the four digit decimal display and the 2048 lamp would light up. The calibrate position of S13 is very useful for testing and calibration.

Three additional switches are provided S14, S15, and S16. These are push button switches which energize relays to simulate capacitance probe levels of 5% for S14, 90% for S15 and S16 is used as a functional check for a full probe. Switch S16 will substract about 5% from a full scale count.

Transistors Q1, Q2, and Q3 and integrated circuits U1, U2, and U3 are used as lamp drivers for the 21 LED indicator lamps.

The 12 bit counter signals drive 12 LED lamp drivers and a binary to BCD converter located on board 2. Integrated circuits A1 thru A8 are used to convert the binary data to BCD data. A1 thru A8 contains a 256 bit read-only memory in each IC. The outputs of the converters go into BCD decoder-drivers A9 thru A12. The decoder drivers drive 4 LED 7 segment readouts DS1 thru DS4 located on board 1.
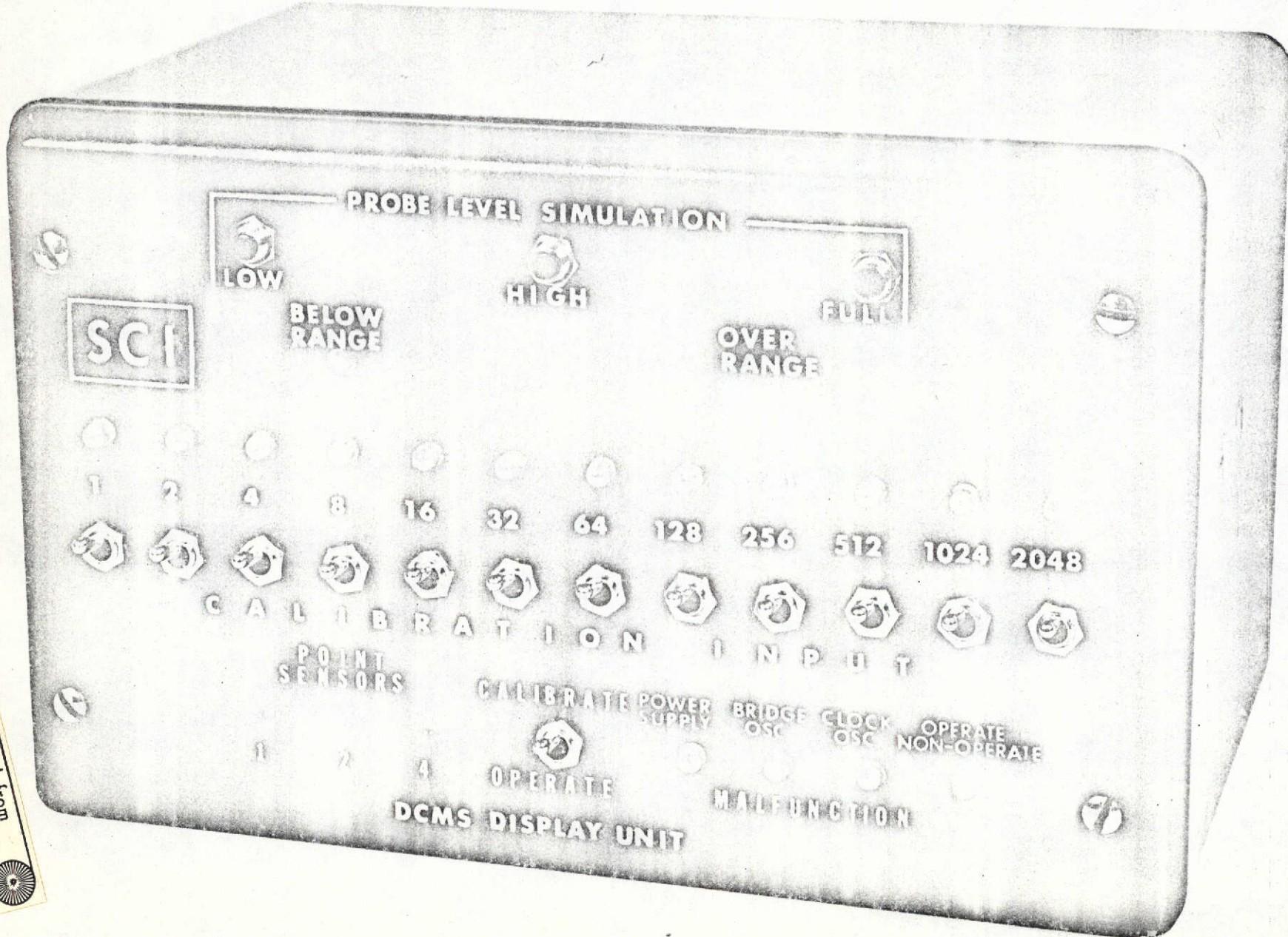
Photograph   DCMS Display Unit

8 7 6 5 4 3 2 1

D

U1
U2
U3

P1
P1
P1

2N2222
2N2222

1K
1K
1K

128 256 512 1024 2048

C

P2   M L K J H G F E D C B A

A1 SN74185A
A2 SN74185A
A3 SN74185A   A4 SN74185A
A5 SN74185A   A6 SN74185A
A7 SN74185A   A8 SN74185A

COUNTER LOAD
COMMON
DET OUT
CHASSIS GND
TEST POINTS

1 2 4 8 16 32 64 128 256 512 1024 2048   OPERATE CALIBRATE

P2   P   R   S   T   U   V   W   Y   Z   AA BB   N   P2

S1   S2   S3   S4   S5   S6   S7   S8   S9   S10   S11   S12   S13

S14   S15   S16   TEST POINTS

+5V
680   680   680

A9 MSD101   A10 MSD101   A11 MSD101   A12 MSD101

LOW   HIGH   FULL

P1   P1

DS1   DS2   S3   DS4

B

A

Several test points are available on the rear panel. These are: Error Signal Low, Error Signal High, ADC/DAC Analog Output, Clock Inhibit, and Clock Sync. Power to operate the Display Unit is +5 volts applied to a jack on the rear panel.

7.0   OPERATING INSTRUCTIONS

Specific operating instructions will depend upon the application of the DCMS. Certain controls, test points, and test equipment are common to all functions and are described in the general operating instructions. Specific operating instructions for three representative functions are given.

7.1   TEST EQUIPMENT

The following basic test equipment, or equivalent, is required as a minimum for proper set up and calibration of the DCMS.

   a)   Wideband dual trace DC oscilloscope

   b)   Power supply - 28 volt $\pm$ 10% @ 1A

   c)   Air capacitor - General Radio type
        1422CB   50 to 1100 pF   2 each

   d)   Air capacitor - General Radio type
        1403-G   10 pF $\pm$ .1%   2 each

   e)   DCMS DISPLAY UNIT

7.1.1   Test Points (Internal)

Internal test points for the point sensor circuit are available on each point sensor board.

7.1.2   Test Points (External)

Various test points are available on test connectors J1 and J2. When the DCMS Display Unit is connected to J1 and J2, these test points are then available on the rear panel of the DCMS Display Unit.
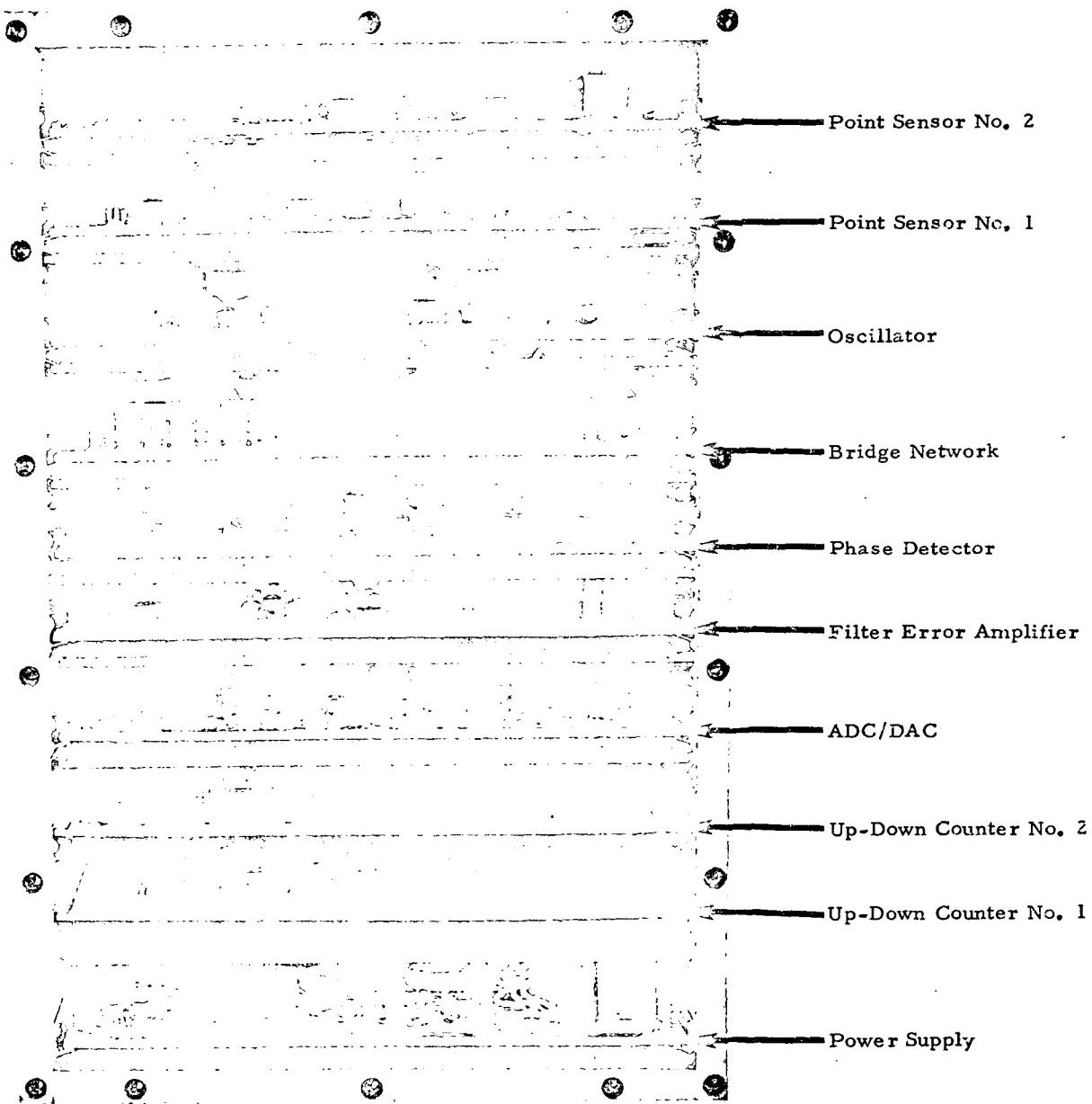
Point Sensor No. 2

Point Sensor No. 1

Oscillator

Bridge Network

Phase Detector

Filter Error Amplifier

ADC/DAC

Up-Down Counter No. 2

Up-Down Counter No. 1

Power Supply

DCMS PW Board Location

ZONE	LTR	REVISIONS		
		DESCRIPTION	DATE	APPROVAL
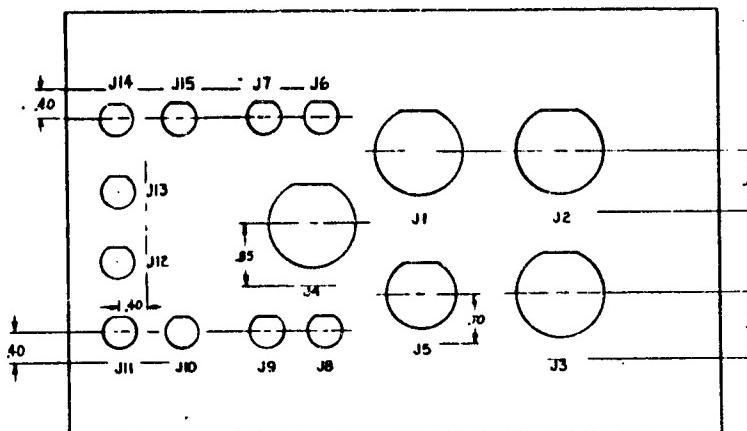
NOTE:
1. ENGRAVE .12 HIGH CHARACTERS PER MIL-STD-130.

J14   J15   J7   J6

.40

J13

J12

.40

.40

J11   J10   J9   J8

J1   J2

J4

J5   J3

.85

.85

.85

.85

.70

2873008-1 SHOWN

			LIST OF MATERIALS OR PARTS LIST					
QTY REQ'D	ITEM NO	NOMENCLATURE OR DESCRIPTION		IDENT. NO. CODE	PART OR IDENT NO	SPEC	MATERIAL OR SPEC	

UNLESS OTHERWISE SPECIFIED

INTERPRET PER MIL-D-1000

THREADS PER MIL-S-7742

REMOVE ALL BURRS AND BREAK ALL SHARP EDGES

IDENTIFY BY BAG AND OR TAG PER MIL STD 130

DIMENSIONS AND TOLERANCES APPLY BEFORE FINAL FINISH

DIMENSIONS ARE IN INCHES

TOLERANCES ON
FRACTIONS DECIMALS ANGLES
.X ±
.XX ± .01
.XXX ±

MATERIAL
MAKE FROM 2873006

FINISH

DEPT SEC	FIG A15
NEXT ASSY	USED ON
APPLICATION	

DR

DSGN

CHK

APPD

PROJ ENG

CONTRACT NO

DESIGN APPROVAL

OTHER APPROVAL

SCI SYSTEMS, INC.
OTHER
HUNTSVILLE ALA
HOUSTON TEXAS
DECATUR ALA

MARKING DETAIL,
COVER, TOP
DCMS

SIZE C	CODE IDENT NO 17981	DWG NO 2873006
SCALE 1/1	UNIT WT	SHEET 1 OF 1

ZONE	LTR	DESCRIPTION	DATE	APPROVAL

POINT SENSOR
● CALIBRATE

● PHASE ADJUST
● DIFFERENTIAL ● ERROR AMP.
BALANCE ADJ. GAIN ADJUST

● ADC GAIN ADJUST

● POINT SENSOR
QUAD

● WINDOW THRESHOLD

LOW LEVEL SIM.
HIGH LEVEL SIM.
IN-PHASE UNKNOWN
QUAD UNKNOWN
FULL PROBE TEST
IN-PHASE REF.
QUAD REF.

T QTY REQD	ITEM NO	NOMENCLATURE OR DESCRIPTION	IDENT NO CODE	PART OR IDENT NO	SPEC	MATERIAL OR NOTE

LIST OF MATERIALS OR PARTS LIST

UNLESS OTHERWISE SPECIFIED			
INTERPRET PER MIL D 1000	DIMENSIONS ARE IN INCHES	DR	
		DSGN	
THREADS PER MIL S 7742	TOLERANCES ON FRACTIONS DECIMALS ANGLES	CHK	
		APPD	
REMOVE ALL BURRS AND BREAK ALL SHARP EDGES		PROJ ENG	
		CONTRACT NO	
IDENTIFY BY BAG AND OR TAG PER MIL STD 130	MATERIAL	DESIGN APPROVAL	
DIMENSIONS AND TOLERANCES APPLY BEFORE FINAL FINISH	FINISH	OTHER APPROVAL	

SCI SYSTEMS, INC. HUNTSVILLE ALA HOUSTON TEXAS DECATUR ALA

SIZE	CODE IDENT NO	DWG NO	
C	17981		
SCALE		UNIT WT	SHEET

NEXT ASSY	USED ON
APPLICATION	

7.2   COMMON SYSTEM ADJUSTMENTS

Five system adjustments are applicable to any function. These are error amplifier bandpass filter, oscillator frequency, demodulation phase, error amplifier gain and window threshold. Three of these, error amplifier bandpass filter, oscillator frequency, and demodulator phase adjust, are set at the time of fabrication and should not be changed.

7.2.1   Error Amplifier Bandpass Filter

This consists of two tuned transformers which are tuned for a peak in error amplifier output at the oscillator frequency. These adjustments are set at the time of fabrication and should not be changed.

7.2.2   Oscillator Frequency

A slug in the oscillator transformer adjusts the frequency to the center of the bandpass of the bandpass filter. This is adjusted for zero phase shift of the error signal thru the bandpass filter, which gives maximum rejection of the in-phase signal in the automatic null quadrature circuit. This adjustment is set at the time of fabrication and should not be changed.

7.2.3   Phase Detector Phase Adjust

A potentiometer is provided to adjust the phase of the drive voltage to a phase shift of 90° and give maximum rejection of quadrature in the in-phase phase detector. This adjustment is set at the time of fabrication and should not be adjusted unless the bridge capacitors are changed for a different range, this adjustment affects the temperature compensation.

7.2.4   Error Amplifier Gain

This adjustment is used to prevent saturation of the error amplifier output

when large capacitance values are being measured. Adjust the gain as high as possible without saturation or excessive noise.

7.2.5 Window Threshold

This potentiometer is adjusted to eliminate up-down count oscillation and to add some noise immunity to the system. Connect oscilloscope to pin f of connector J4, phase detector output. Turn the window threshold potentiometer fully counterclockwise (about 20 turns). Adjust the unknown capacitor for +1 volt out of the phase detector. Note the readout count, slowly turn the window threshold potentiometer clockwise until the readout increases 1 count. This sets the threshold to $\pm$ 1 volt and is only a typical setting. A full scale range of 5 pF would require a lower threshold t.. a full scale range of 1000 pF.

7.3   SET-UP AND CALIBRATION

The following instructions are for three types of uses of which the DCMS is capable. Distinct similarity of the three cases are to be noted. Referring to Figure 2 for component location, to measure absolute capacitance the bridge components are set up as follows:

C15-C16 = unknown capacitance external to the unit

C19-C20 = 0

C21-C22 = Base reference set at initial value of C15-C16

C17-C18 = Range reference set at total change of C15-C16

To measure Capacitance ratio:

C15-C16 = unknown capacitance subject to several variables only one of which is to be measured.

C17-C18 = external reference capacitor subject to all variables of C15-C16 except the one to be measured.

C19-C20 = base or initial value of C17-C18

C21-C22 = base or initial value of C15-C16

To measure capacitance difference:

C15 and C21 = external capacitors for which the difference is to be resolved.

C19-C20 = 0

C17-C18 - absolute reference equal to twice the expected full-scale difference between C15 and C21

C16 = capacitance in parallel with C15 = t= 1/2C17-C18.

The null balance adjustment is the operation of reducing the intial values of I and I_2 to zero. Four variable voltage sources are provided to accomplish this. A capacitor located on the bridge board connected between a variable voltage source and the bridge node will inject a vector current which can be varied along the imaginary axis. A resistor, also located on the bridge board, will inject a vector current along the real axis. Thus, any vector current can be injected into the node by varying the two voltage sources and selecting the values of the capacitor and resistor. These adjustments are labeled "unknown-in-phase" (capacitor) "unknown-quadrature" (resistor) for the unknown node, and "reference-in-phase" and "reference-quadrature" for the reference node.

In some functions it is desirable to have internal transfer capacitors which can, on command, be connected to simulate changes in the unknown and the reference capacitors. For this purpose three relays are provided having single-pole double-throw operation. Fixed capacitors on the bridge board can furnish fractional scale simulation upon remote command. The adjustments are labeled "probe level simulation (low and high)" and "full probe test".

7.3.1   Absolute Capacitance Set-Up and Calibration

To measure an absolute capacitance from 100 pf to 120 pf use the following procedure.

7.3.1.1   Preparation

A 20 pf NPO reference capacitor should be installed for C17-C18. A total of 100 pf NPO capacitance should be installed for C21-C22. A combined total of 22 pf NPO for C6-C7. C8 = 15 pf NPO. Total of C9 should be 330 pf NPO and C10 = to 27 pf NPO. C13 = 68 pf NPO. C11 = 27 pf NPO. C14 = 22 pf NPO. All these components are located on the bridge network board, schematic 2873032.

7.3.1.2 Null Balance and Calibration

1. Connect the cables from the DCMS test set to J1 and J2 for operation of the DCMS Test Set. Connect +5 volt to the test set.

2. Connect the +28V primary supply.

3. Apply power.

4. Turn the calibrate/operate switch on the DCMS Display Test Set to Calibrate.

5. Connect one oscilloscope probe to the test set "Error Amplifier" output jack.

6. Connect the other probe to pin f of connector J4, the phase detector output.

7. Arrange to trigger the scope externally from the excitation connector J9.

8. Connect a 100 pf variable air capacitor to connectors J6 and J8.

9. Set binary control switches to 00---00. Vary the "unknown quadrature" and "unknown-in-phase" controls to obtain minimum error output and zero output out of the phase detector.

10. Adjust the "Error amplifier gain adjust" for as high a gain as possible without saturation or excessive noise.

11. Adjust the "window threshold" control to eliminate up-down count oscillation and excessive jitter of the counter. See 4.2.5.

12. Adjust the "Phase adjust" control for best quadrature rejection. Vary the "unknown quadrature" control plus-or-minus 1 or 2 turns from the null while adjusting the "phase adjust" control until the "unknown quadrature" control no longer has an effect

on the output of the phase detector. The demodulator phase is thereby set to reject the unwanted quadrature vector of bridge error. Readjust "unknown in-phase" and "unknown quadrature" for minimum error.

13. Temperature compensation must be done after step 12. The temperature coefficient of bridge capacitors C21-C22 are selected to have a slightly positive coefficient to compensate for the basic negative drift of the DCMS.

14. Set the binary control switches to 111110100000 and the variable capacitor to 120 pf. Adjust reference-in-phase and reference quadrature controls for minimum error output and zero output of the phase detector. ADC gain adjust control R88 schematic 2873026, may be used as a fine adjust for getting zero volts out of the phase detector.

15. Temperature compensation of full scale is next. This is done with thermistor network R91, 92, R93, R94 and R95 located on the ADC board, schematic 2873026. R91 is selected to compensate for gain changes in the ADC and Bridge circuit. A typical value might be about 100K ohms. Repeat step 14.

16. Set the Calibrate/Operate switch to operate. Set the variable capacitor to 100 pf, the counter readout should read zero.

17. Push the Low Simulate pushbutton on the DCMS Display Unit. Adjust the Low Level Simulator Control for a readout count of 200.

18. Push the High Level Simulator pushbutton switch and adjust the High Level Simulator Control for a readout count of 3600.

19. Set the variable capacitor to 120.475 pf. Push the Full Probe Test pushbutton on the test set and adjust the Full Probe Test Control for a readout count of 3900.

20. The unit is now calibrated such that the binary output is proportional to the unknown capacitance from 100.000 pf to 120.475 pf maximum.

7.3.2 Capacitance Ratio Set-Up and Calibration

To measure a capacitance ratio of 20:1 with an unknown initial capacitance of 300 pf and an initial capacitance of 15 pf for the external reference capacitor. At the start of measurement, the external reference capacitor will increase 20 pf. The unknown capacitor will increase 400 pf for full scale.

7.3.2.1 Preparation

A 20 K ohm .005% resistor should be installed for R67 and a 1050 ohm .005% resistor for R87 on the ADC board schematic 2873026. The following are located on the bridge network board. A 300 pf NPO capacitor should be installed for C21. A 15 pf NPO capacitor should be installed for C19-C20. All the following capacitors should be NPO. C6-C7 = 400 pf. C8 = 62 pf. C9 - 7600 pf. C10 = 560 pf. C13 = 1300 pf. C11 = 560 pf. C14 = 22 pf.

7.3.2.2 Null Balance and Calibration

1. Connect cables from the DCMS Display Unit to DCMS J1 and J2 for operation of the test set. Connect +5 volts to the test set.

2. Connect the +28 volt supply.

3. Apply power.

4. Set the calibrate/operate switch on the test set to calibrate.

5. Connect one oscilloscope probe to the test set error amplifier output jack.

6. Connect the other probe to pin f of connector J4, the phase detector output.

7. Arrange to trigger the scope externally from excitation connector J9.

8. Connect a 50-1100 pf capacitor to connectors J6 and J8. Set the capacitor to 300 pf.

9. Set binary control switches to 00---00. Vary the unknown-quadrature and unknown-in-phase controls to obtain minimum error output and zero output out of the phase detector.

10. Adjust the error amplifier gain adjust for as high a gain as possible without saturation or excessive noise.

11. Adjust the window threshold control to eliminate up-down count oscillation and excessive jitter of the counter. See 4.2.5.

12. Adjust the phase adjust control for quadrature rejection. Vary the unknown quadrature control plus-or-minus 1 or 2 turns from the null while adjusting the phase adjust control until the unknown quadrature control no longer has an effect on the output of the phase detector. The demodulator phase is thereby set to reject the unwanted quadrature vector of bridge error. Readjust unknown-in-phase and unknown quadrature for minimum error.

13. Temperature compensation must be done after step 12. The temperature coefficient of bridge capacitor C21-C22 (300 pf) is selected to have the proper temperature coefficient to cancel the drift of the DCMS.

14. Connect a 5 to 110 pf air variable capacitor to J7 and J8. Set the capacitor to 15 pf. Set all of the binary control switches high for a readout of 4095.

15. Adjust reference-in-phase and reference quadrature controls for minimum error output and zero output of the phase detector.

16. Set the unknown capacitor to 700 pf and the reference capacitor to 35 pf. Set the operate/calibrate switch to operate.

17. Adjust ADC gain adjust control R88 (schematic 2873026) for a readout count of 4000. If R88 does not have enough range, resistors R82 and R96 may be changed to bring R88 on center range.

18. If excessive quadrature occurs somewhere over the 300 pf to 700 pf range, R32 may be lowered to reduce the quadrature error.

19. Temperature compensation of full scale is next. This is done with thermistor network R91, R92, R93, R94 and R95 located on the ADC board, schematic 2873026. R91 is selected to compensate for gain changes in the ADC and bridge circuit. A Typical value might be about 100 K ohms.

20. Set the unknown capacitor to 300 pf. The counter readout should read zero.

21. Push the Low-Simulate pushbutton on the DCMS Display Unit. Adjust the Low Simulate control for a readout count of 200.

22. Push the High Level Simulate pushbutton switch and adjust the High Level Simulate control for a readout count of 3600.

23. Set the unknown capacitor to 709.5 pf, the readout should read 4095. Push the Full Probe Test pushbutton on the test set and adjust the Full Probe Test control for a readout count of 3900.

24. The DCMS Unit is now calibrated to read capacitance ratio with a ratio of 20:1 full scale. The unknown capacitance range is 300 pf to 700 pf and the external reference changes from an initial value of 15 pf to 35 pf when measurement starts.

7.3.3   Capacitance Difference Set-Up and Calibration

To measure the capacitance difference of two capacitors with a nominal value of 400 pf to 800 pf with a capacitance difference of ± 20 pf, use the following procedure.

7.3.3.1 Preparation

A 870 pf NPO capacitor should be installed in C24 for a reference capacitor. The following capacitors should be NPO temperature coefficient. C7 = 47 pf. C8 = 22 pf. C10 = 68 pf. C13 = 47 pf. C11 – 47 pf. C14 = 47 pf. C23 = 470 pf. R23 = 24K. R25 = 16K. R32 = 3.9K. A jumper wire should be soldered on the terminals to connect the wiper of potentiometer R1 Differential Balance Adjust to bridge-ground printed circuit pin No. 33. All these components are located on the bridge network board, schematic 2873032.

7.3.3.2 Null Balance and Calibration

1. Connect the cables from the DCMS Display Unit to DCMS J1 and J2 for operation of the DCMS display unit. Connect +5 volts to the display unit.

2. Connect the +28 V primary supply.

3. Apply power.

4. Turn the calibrate/operate switch on the DCMS Display Test Set to calibrate.

5. Connect one oscilloscope probe to the test set error amplifier output jack.

6. Connect the other probe to pin f of connector J4, the phase detector output.

7. Arrange to trigger the scope externally from excitation connect J9.

8. Set binary control switches to 00---00. Vary the unknown-in-phase and unknown quadrature controls to obtain minimum error output and zero output out of the phase detecotr.

9. Adjust the error amplifier gain adjust for as high a gain as possible without saturation or excessive noise.

10. Adjust the window threshold control to eliminate up-down count oscillation and excessive jitter of the counter. See 4.2.5.

11. Connect one 50 to 100 pf capacitor to J6 and J8 and another one to J9 and J6. Set both capacitors to 800 pf.

12. Adjust R1 Differential Balance Adjust and unknown quadrature to obtain minimum error output. Then adjust unknown in-ph..se for zero output out of the phase detector. Do not change R1 again.

13. Adjust the phase adjust control for best quadrature rejection. Vary the unknown quadrature control plus-or-minus 1 or 2 turns from the null while adjusting the phase adjust control until the unknown quadrature control no longer has an effect on the output of the phase detector. The detector phase is thereby set to reject the unwanted quadrature vector of bridge error. Readjust unknown quadrature for minimum error.

14. Set the binary control switches to 111110100000 and the E+ variable capacitor to 820 pf and the E- capacitor to 780 pf. Adjust reference-in-phase and reference quadrature controls for minimum error output and zero output of the phase detector. ADC gain adjust control R88, schematic 2873026, may be used

15. Set both capacitors to 800 pf and set the calibrate/operate switch to operate, the counter readout should read zero.

16. Connect + 5 volts to pin e of connector J4 to energize the Full Probe Test relay. Adjust the Full Probe Test control for a readout of 2000.

17. Adjust High Level Simulate control for a readout count of 1800 while depressing the High Level Simulate pushbutton.

18. Push the Low Simulate pushbutton on the DCMS Display Unit. Adjust the Low Level Simulate control for a readout count of 2200.

19. Disconnect +5 volts from pine e of J4. With both capacitors set to 800 pf, adjust unknown in-phase for zero count and zero phase detector output.

20. Repeat steps 14, 15, 16, 17, 18 and 19.

21. Temperature compensation must be done after step 20. The temperature coefficient of bridge capacitors C21-C22 and C15-C16 are selected to compensate for the drift of the DCMS. Do not change the adjustment of R1 the differential balance adjust. Select capacitors for C15-C16 and C21-C22 to be equal with a nominal value of 100 pf. The C21-C22 combination should be NPO and the C15-C16 combination should have a negative temperature coefficient to cancel the drift of the DCMS. The two combinations should be equal at room temperature. Capacitors C15-C16 could consist of a small value NPO and a large value of silvered mica with a total value of 100 pf. The correct combination of NPO and negative mica must be found to compensate for drift.

22. Repeat step 14.

23. Temperature compensation of full scale is next. This is done with the thermistor network R91, R92, R93, R94 and R95 located on the ADC board, schematic 2873026. R91 is selected to compensate for gain changes in the ADC and bridge circuit. A typical value might be about 24 K ohms.

24. Adjust the unknown in-phase control for zero count and zero phase detector output.

25. Repeat steps 14, 15, 16, 17 and 18.

26. The DCMS is now calibrated to read the difference of two capacitors with 1000--00 indicating no difference, 111110100000 indicating 20 pf difference and 000---00 indicating 20 pf difference.

TROUBLESHOOTING CHART

	Sympton	Probable Cause	Remedy
1.	Bridge balances slowly	Clock sync disconnected. Bad sync amplifier U9 on Up/Down counter board No. 2, 2873047	Connect sync, trouble-shoot U9 and surrounding circuit
2.	Counts in one direction only	Phase Detector No. 2873035	Check pin f of J4 output of ± 3 volts in manual operation. If OK, remove board and check operation of U8 and U9. If Ok go to step 2.
2a	Counts in one direction only	Counter board No. 2, 2873047	Check operation of gate U8.
3.	DCMS does not count up or down	Counter Schematic 2873047	Check operation of phase detector for ± 3 volts output on pin f of J4 in manual mode. If OK check counter for trouble. If defective, go to step 3a.
3a	DCMS does not count up or down	Phase Detector Schematic 2873035	Check error amplifier output pin T of J1. If OK, check the phase detector board. If not OK, go to 3b.
3b	DCMS does not count up or down	Error amplifier Schematic 2873050	Check error amplifier outpu pin Z of J1. If OK, trouble is with Q2 amplifier circuit or U1 or U2 amplifier circuit. If no signal is present, go to step 3c.
3c	DCMS does not count up or down	ADC/DAC Schematic 2873026	Check manual operation of Analog output. Set switches for 4095 count, output shocl, be about +5 volts. Set switches for 2048, output should be about +2.5 volts. Set the switches to 000, the output should be about zero volts. If the above test is OK, the probable cause is in the bridge board.

7.3.4   Point Sensor Set-Up and Calibration

The point sensor is set up at the time of fabrication to signal condition unknown capacitors of 5.5 pf to 7.5 pf. However, the typical over-range limits are 4.5 pf to 8.6 pf. No temperature compensation is required.

7.3.4.1   Preparation

Connect a .5 pf to 11 pf air variable capacitor to DCMS connector J8 and to J12.

7.3.4.2   Null Balance and Calibration

1.   Connect the cables from the DCMS test set to J1 and J2 for operation of the DCMS Disply Unit. Connect +5 volts to the display unit.

2.   Connect the +28 volt primary supply.

3.   Apply power.

4.   Connect an oscilloscope probe to TP 5 on point sensor signal conditioner board No. 1, schematic No. 2873041. Refer to **Point Sensor No. 1** photograph for location of test points 1 thru 6.

5.   Set the variable capacitor to 5.5 pf. Adjust quad adjust R7 and calibrate R8 controls for minimum error output on TP 5.

6.   Turn the calibrate potentiometer counter clockwise until the "1" and "2" lamps on the display unit go out. These lamps are located in the lower left corner. If the "1" and "2" lamps were already dark, proceed to step 7.

7.   Very slowly turn the calibrate control clockwise until the "1" and "2" lamps just light.

8.   Turn the capacitor to 5.0 pf and push the low simulate pushbutton. The "1" and "2" lamp should light.

9. Set the capacitor to 6 pf, push the high simulate pushbutton. The "1" and "2" lamps should go out.

10. All six point sensor signal conditioners are now calibrated to indicate 5.5 pf. Schematic 2873044 shows point sensor signal conditioner No. 2. Test points 1 through 6 for point sensor No. 2 are shown in Point Sensor No. 2 photograph.